DOCUMENT RESUME

ED 246 221 CE 039 206

TITLE Electronic Principles VI, 7-10. Military Curriculum Materials for Vocational and Technical Education.

INSTITUTION Air Force Training Command, Keesler AFB, Miss.; Ohio State Univ., Columbus. National Center for Research in Vocational Education.

SPONS AGENCY Department of Education, Washington, DC.

PUB DATE 75

NOTE 339p.; For related documents, see CE 039 201-210.

PUB TYPE Guides - Classroom Use - Materials (For Learner) (051) -- Guides - Classroom Use - Guides (For Teachers) (052)

EDRS PRICE MF01/PC14 Plus Postage.

DESCRIPTORS Behavioral Objectives; Course Content; Course Descriptions; *Electric Circuits; *Electronic Equipment; *Electronics; Individualized Instruction; Learning Activities; Learning Modules; Pacing; Postsecondary Education; Programed Instructional Materials; Secondary Education; *Technical Education

IDENTIFIERS *Electric Generators; Military Curriculum Project; *Solid State (Electronics)

ABSTRACT

This sixth of 10 blocks of student and teacher materials for a secondary/postsecondary level course in electronic principles comprises one of a number of military-developed curriculum packages selected for adaptation to vocational instruction and curriculum development in a civilian setting. Prerequisites are the previous blocks. This block on solid state wave generating and wave shaping circuits contains nine modules covering 68 hours of instruction on principles of oscillations (5 hours), solid state LC oscillators (8), solid state RC oscillators (5), solid state frequency multipliers (4), solid state pulsed and block oscillators (8), solid state multivibrators (]2), solid state sawtooth generators (8), solid state trapezoidal generators (7), and solid state limiters and clampers (11). Printed instructor materials include a plan of instruction detailing the units of instruction, duration of the lessons, criterion objectives, and support materials needed. Student materials include a student text; nine guidance packages containing objectives, assignments, review exercises and answers for each module; and two programmed texts. A digest of the modules in the block is provided for students who need only to review the material. Designed for self- or group-paced instruction, the material can be adapted for individualized instruction. Additional print and audiovisual materials are recommended but not provided. (YLB)

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MILITARY CURRICULUM MATERIALS

The military-developed curriculum materials in this course package were selected by the National Center for Research in Vocational Education Military Curriculum Project for dissemination to the six regional Curriculum Coordination Centers and other instructional materials agencies. The purpose of disseminating these courses was to make curriculum materials developed by the military more accessible to vocational educators in the civilian setting.

The course materials were acquired, evaluated by project staff and practitioners in the field, and prepared for dissemination. Materials which were specific to the military were deleted, copyrighted materials were either omitted or approval for their use was obtained. These course packages contain curriculum resource materials which can be adapted to support vocational instruction and curriculum development.

The National Center Mission Statement

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- Generating knowledge through research
- Developing educational programs and products
- Evaluating individual program needs and outcomes
- Installing educational programs and products
- Operating information systems and services
- Conducting leadership development and training programs

FOR FURTHER INFORMATION ABOUT
Military Curriculum Materials
WRITE OR CALL

Program Information Office
The National Center for Research in Vocational Education
The Ohio State University
1960 Kenny Road, Columbus, Ohio 43210
Telephone: 614/486-3655 or Toll Free 800/848-4815 within the continental U.S. (except Ohio)

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FOR RESEARCH IN VOCATIONAL EDUCATION
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Military Curriculum Materials for Vocational and Technical Education

Information and Field Services Division

The National Center for Research in Vocational Education

Military Curriculum Materials Dissemination Is . . .

an activity to increase the accessibility of military-developed curriculum materials to vocational and technical educators.

This project, funded by the U.S. Office of Education, includes the identification and acquisition of curriculum materials in print form from the Coast Guard, Air Force, Army, Marine Corps and Navy.

Access to military curriculum materials is provided through a "Joint Memorandum of Understanding" between the U.S. Office of Education and the Department of Defense.

The acquired materials are reviewed by staff and subject matter specialists, and courses deemed applicable to vocational and technical education are selected for dissemination.

The National Center for Research in Vocational Education is the U.S. Office of Education's designated representative to acquire the materials and conduct the project activities.

Project Staff:

Wesley E. Budke, Ph.D., Director
National Center Clearinghouse

Shirley A. Chase, Ph.D.
Project Director

What Materials Are Available?

One hundred twenty courses on microfiche (thirteen in paper form) and descriptions of each have been provided to the vocational Curriculum Coordination Centers and other instructional materials agencies for dissemination.

Course materials include programmed instruction, curriculum outlines, instructor guides, student workbooks and technical manuals.

The 120 courses represent the following sixteen vocational subject areas:

- Agriculture
- Aviation
- Building & Construction Trades
- Clerical Occupations
- Communications
- Drafting
- Electronics
- Engine Mechanics
- Food Service
- Health
- Heating & Air Conditioning
- Machine Shop
- Management & Supervision
- Meteorology & Navigation
- Photography
- Public Service

The number of courses and the subject areas represented will expand as additional materials with application to vocational and technical education are identified and selected for dissemination.

How Can These Materials Be Obtained?

Contact the Curriculum Coordination Center in your region for information on obtaining materials (e.g., availability and cost). They will respond to your request directly or refer you to an instructional materials agency closer to you.

CURRICULUM COORDINATION CENTERS

EAST CENTRAL
Rebecca S. Douglass
Director
100 North First Street
Springfield, IL 62777
217/782-0759

MIDWEST
Robert Patton
Director
1515 West Sixth Ave.
Stillwater, OK 74704
405/377-2000

NORTHEAST
Joseph F. Kelly, Ph.D.
Director
225 West State Street
Trenton, NJ 08625
609/292-6562

NORTHWEST
William Daniels
Director
Building 17
Airdustrial Park
Olympia, WA 98504
206/753-0879

SOUTHEAST
James F. Shill, Ph.D.
Director
Mississippi State University
Drawer DX
Mississippi State, MS 39762
601/325-2510

WESTERN
Lawrence F. H. Zane, Ph.D.
Director
1776 University Ave.
Honolulu, HI 96822
808/948-7834

ELECTRONIC PRINCIPLES VI

Table of Contents

Course Description Page 1

Plan of Instruction Page 3

Volume VI

Solid State Wave Generating and Wave Shaping Circuits - Student Text Page 31

Modules 42-50 - Digest Page 123

Module 42

Principles of Oscillations - Guidance Package Page 145

Module 43

Solid State LC Oscillators - Guidance Package Page 151

Module 44

Solid State RC Oscillators - Guidance Package Page 166

Module 45

Solid State Frequency Multipliers - Guidance Package Page 196

Module 46

Solid State Pulsed and Blocking Oscillators - Guidance Package Page 201

Module 47

Solid State Multivibrators - Guidance Package Page 212

Solid State Multivibrators - Programmed Text Page 262

Module 48

Solid State Sawtooth Generators - Guidance Package Page 314

Module 49

Solid State Trapezoidal Generators - Guidance Package Page 328

-continued-

Module 59

Solid State Trapezoidal Waveform Generator - Programmed Text Page 342

Module 50

Solid State Limiters and Clampers Guidance Package Page 356

ELECTRONIC PRINCIPLES VI

Classroom Course 7-10

Developed by:

United States Air Force

Development and Review Dates:

November 6, 1975

D.O.T. No.:
003.081

Occupational Area:

Electronics

Target Audiences:

Grades 11-adult

Print Pages:

367

Cost:

$7.50

Availability:

Military Curriculum Project, The Center for Vocational Education, 1960 Kenny Rd., Columbus, OH 43210

Contents:	Type of Materials:						Instructional Design:				Type of Instruction:		
	Lesson Plans:	Programmed Text:	Student Workbook:	Handouts:	Text Materials:	Audio-Visuals:	Performance Objectives:	Tests:	Review Exercises:	Additional Materials Required:	Group Instruction:	Individualized:	
			No. of pages										
Block VI – *Solid State Wave Generating and Wave Shaping Circuits*													
Module 42 – **Principles of Oscillations**	●		6		●	★	●	★	●		●	●	
Module 43 – **Solid State LC Oscillators**	●		13		●	★	●	★	●	★	●	●	
Module 44 – **Solid State RC Oscillators**	●		30		●	★	●	★	●	★	●	●	
Module 45 – **Solid State Frequency Multipliers**	●		6		●		●	★	●		●	●	
Module 46 – **Solid State Pulsed and Blocking Oscillators**	●		11		●		●	★	●		●	●	
Module 47 – **Solid State Multivibrators**	●	●	40		●		●	★	●		●	●	
Module 48 – **Solid State Sawtooth Generators**	●		14		●	★	●	★	●	★	●	●	
Module 49 – **Solid State Trapezoidal Generators**	●	●	14		●		●	★	●	★	●	●	
Module 50 – **Solid State Limiters and Clampers**	●	●	27		●	★	●	★	●	★	●	●	

★ **Materials are recommended but not provided.**

11

Expires July 1, 1978

Course Description:

This block is the sixth of a ten-block course providing training in electronic principles, use of basic test equipment, safety practices, circuit analysis, soldering, digital techniques, microwave principles and troubleshooting basic circuits. Prerequisites to this block are Blocks I through V covering DC circuits, AC circuits, RCL circuits, solid state principles, and solid state power supplies and amplifiers. Block VI—*Solid State Wave Generating and Wave Shaping Circuits* contains nine modules covering 68 hours of instruction over the principles of oscillations, solid state oscillators, multipliers, multivibrators, sawtooth generators, trapezoidal generators, limiters and clampers. The module topics and respective hours follow:

Module 42 — **Principles of Oscillations** (5 hours)
Module 43 — **Solid State LC Oscillators** (8 hours)
Module 44 — **Solid State RC Oscillators** (5 hours)
Module 45 — **Solid State Frequency Multipliers** (4 hours)
Module 46 — **Solid State Pulsed and Block Oscillators** (8 hours)
Module 47 — **Solid State Multivibrators** (12 hours)
Module 48 — **Solid State Sawtooth Generators** (8 hours)
Module 49 — **Solid State Trapezoidal Generators** (7 hours)
Module 50 — **Solid State Limiters and Clampers** (11 hours)

This block contains both teacher and student materials. Printed instructor materials include a plan of instruction detailing the units of instruction, duration of the lessons, criterion objectives, and the support material needed. Student materials consist of a student text used for all the modules; nine guidance packages containing objectives, assignments, review exercises and answers for each module ; and two programmed texts on solid state multivibrators and solid state trapezoidal waveform generators. A digest of modules 42–50 for students who have background in these topics and only need to review the major points of instruction is also included.

This material is designed for self- or group-paced instruction to be used with the remaining nine blocks. Most of the materials can be adapted for individualized instruction. Some additional military manuals and commercially produced texts are recommended for reference, but are not provided. Audiovisuals suggested for use with the entire course consits of 143 videotapes which are not provided.

3

POI 3AQR30020-1

PLAN OF INSTRUCTION
(Technical Training)

ELECTRONIC PRINCIPLES
(Modular Self-Paced)

AIR TRAINING COMMAND

KEESLER TECHNICAL TRAINING CENTER
6 November 1975 - Effective 6 January 1976 with Class 760106
Volume 6

7-10

DEPARTMENT OF THE AIR FORCE
USAF Sch of Applied Aerosp Sci (ATC)
Keesler Air Force Base, Mississippi 39534

PLAN OF INSTRUCTION 3AQR30020-1
6 November 1975

FOREWORD

1. PURPOSE: This publication is the plan of instruction (POI) when the pages shown on page A are bound into a single document. The POI prescribes the qualitative requirements for Course Number 3AQR30020-1, Electronic Principles (Modular Self-Paced) in terms of criterion objectives and teaching steps presented by modules of instruction and shows duration, correlation with the training standard, and support materials and guidance. When separated into modules of instruction, it becomes Part I of the lesson plan. This POI was developed under the provisions of ATCR 50-5, Instructional System Development, and ATCR 52-7, Plans of Instruction and Lesson Plans.

2. COURSE DESIGN/DESCRIPTION. The instructional design for this course is Modular Scheduling and Self-Pacing; however, this POI can also be used for Group Pacing. The course trains both non-prior service airmen personnel and selected re-enlistees for subsequent entry into the equipment oriented phase of basic courses supporting 303XX, 304XX, 307XX, 309XX and 328XX AFSCs. Technical Training includes electronic principles, use of basic test equipment, safety practices, circuit analysis, soldering, digital techniques, microwave principles, and troubleshooting of basic circuits. Students assigned to any one course will receive training only in those modules needed to complement the training program in the equipment phase. Related training includes traffic safety, commander's calls/briefings and end of course appointments.

3. TRAINING EQUIPMENT. The number shown in parentheses after equipment listed as Training Equipment under SUPPORT MATERIALS AND GUIDANCE is the planned number of students assigned to each equipment unit.

4. REFERENCES. This plan of instruction is based on Course Training Standard KE52-3AQR30020-1, 27 June 1975 and Course Chart 3AQR30020-1, 27 June 1975.

FOR THE COMMANDER

W. H. HORNE, Colonel, USAF
Commander
Tech Tng Gp Prov, 3395th

OPR: Tech Tng Gp Prov, 3395th
DISTRIBUTION: Listed on Page A

5

PLAN OF INSTRUCTION/LESSON PLAN PART I

NAME OF INSTRUCTOR	COURSE TITLE Electronic Principles
BLOCK NUMBER VI	BLOCK TITLE Solid State Wave Generating and Wave Shaping Circuits

1 COURSE CONTENT	2 DURATION (Hours)
1. Principles of Oscillations (Module 42)	5 (4/1)

1. Principles of Oscillations (Module 42)

a. From a list of statements, select the statement(s) that describe(s) the requirements for sustaining oscillations at a particular frequency. CTS: 5f(1), 5f(2), 5f(3) Meas: W

- (1) Amplifier
  - (a) Common Emitter
  - (b) Common Base
  - (c) Common Collector
- (2) Frequency Determining Device
  - (a) LC Tank Circuit
  - (b) RC Circuit
  - (c) Crystal
- (3) Regenerative Feedback
  - (a) Inductive
  - (b) Capacitive
  - (c) RC Network

SUPERVISOR APPROVAL OF LESSON PLAN (PART II)

SIGNATURE	DATE	SIGNATURE	DATE

PLAN OF INSTRUCTION NO. 3AQR30020-1	DATE 20 November 1975	PAGE NO. 47

ATC FORM APR 75 133 ATC Keesler 6-1029 REPLACES ATC FORMS 337, MAR 73, AND 770, AUG 72, WHICH WILL BE USED.

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SUPPORT MATERIALS AND GUIDANCE

Student Instructional Materials
KEP-GP-42, Principles of Oscillations
KEP-ST-VI, Solid State Wave Generating and Wave Shaping Circuits
KEP-110

Audio Visual Aids
TVK 30-513, Characteristics of Crystals
TVK 30-536, Introduction to LC Oscillators

Training Methods
Discussion (4 hrs) and/or Programmed Self Instruction
CTT Assignment (1 hr)

Instructional Guidance
Make specific objective assignments to be completed during CTT time in KEP-GP-42. Stress the three requirements for sustaining oscillations at a specific frequency and elaborate on the methods of satisfying these requirements.

7

PLAN OF INSTRUCTION/LESSON PLAN PART I

NAME OF INSTRUCTOR	COURSE TITLE
	Electronic Principles

BLOCK NUMBER	BLOCK TITLE
VI	Solid State Wave Generating and Wave Shaping Circuits

1 COURSE CONTENT	2 DURATION (Hours)
2. Solid State LC Oscillators (Module 43)	8 (6/2)
a. From a schematic diagram of any one of the following oscillator circuits, select the components that comprise the feedback loop, frequency determining device, forward bias network, and frequency adjustment: Series Hartley; Shunt Hartley; Colpitts; Clapp; Butler. CTS: 5f(1), 5f(3) Meas: W	(3)

2. Solid State LC Oscillators (Module 43)

a. From a schematic diagram of any one of the following oscillator circuits, select the components that comprise the feedback loop, frequency determining device, forward bias network, and frequency adjustment: Series Hartley; Shunt Hartley; Colpitts; Clapp; Butler. CTS: 5f(1), 5f(3) Meas: W

(1) Series Hartley

(a) Identify the schematic diagram.

(b) Purpose of each component

(c) Explain operation to include

1 regenerative feedback path.

2 regenerative feedback amplitude versus location of the tap on the coil.

3 frequency determining device.

4 tuning.

(d) Identify phase shift requirements for feedback.

(2) Shunt Hartley

(a) Identify the schematic diagram.

(b) Purpose of each component

(c) Explain operation in terms of

1 regenerative feedback path.

SUPERVISOR APPROVAL OF LESSON PLAN (PART II)

SIGNATURE	DATE	SIGNATURE	DATE

PLAN OF INSTRUCTION NO.	DATE	PAGE NO.
3AQR30020-1	20 November 1975	49

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2 frequency determining device.

3 feedback amplitude.

4 tuning.

(d) Identify phase shift requirements for feedback.

(3) Colpitts

(a) Identify the schematic diagram.

(b) Purpose of each component

(c) Explain operation in terms of

1 regenerative feedback path.

2 regenerative feedback amplitude.

3 frequency determining device.

4 tuning.

5 reduced effect of transistor interelement capacitance.

(d) Explain that phase shifting is unnecessary for regenerative feedback.

(4) Clapp

(a) Identify the schematic diagram.

(b) Purpose of each component

(c) Explain operation in terms of

1 frequency determining device.

2 tuning.

(d) Explain that phase shifting is unnecessary for regenerative feedback.

(5) Butler

(a) Identify the schematic diagram.

(b) Purpose of each component

(c) Explain operation in terms of

COURSE CONTENT

1 feedback path.

2 frequency determining device.

3 stability.

(d) Explain that phase shifting is unnecessary for regenerative feedback.

b. Given a list of statements, select the statement(s) which describe(s) the effect of varying the output load on an LC tank circuit. CTS: 5f(1) Meas: W (.5)

(1) Explain the meaning of load and load resistance.

(2) Explain the effect of varying load on

(a) regenerative feedback.

(b) circuit Q.

(c) bandwidth.

(d) frequency stability.

c. Given a list of statements, select the statement(s) which describe(s) the purpose of a buffer amplifier. CTS: 5f(1) Meas: W. (.5)

(1) Interaction between the oscillator and load.

d. Given a trainer, multimeter and oscilloscope, measure the change in output amplitude and frequency for a given change in load at the output of an LC oscillator circuit within ± 10 percent accuracy. CTS: 2a, 5f(1) Meas: PC (1)

e. Given a trainer, multimeter and oscilloscope, measure the change in output amplitude and frequency between a maximum and minimum load with a buffer amplifier inserted between LC oscillator output and the load within ± 10 percent accuracy. CTS: 2a, 5f(1) Meas: PC (1)

SUPPORT MATERIALS AND GUIDANCE

Student Instructional Materials
KEP-GP-43, Solid State LC Oscillators
KEP-ST-VI
KEP-110

Audio Visual Aids
TVK 30-556, Oscillators, TSTR Hartley, Colpitts and EOC

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PLAN OF INSTRUCTION/LESSON PLAN PART I (Continuation Sheet)

COURSE CONTENT

Training Equipment
Hartley Oscillator and Buffer Amplifier Trainer DD6097 (1)
Oscilloscope (1)
Multimeter (1)
Transistor Circuit Power Supply 4649 (1)

Training Methods
Discussion (4 hrs) and/or Programmed Self Instruction
Performance (2 hrs)
CTT Assignments (2 hrs)

Multiple Instructor Requirements
Safety, Equipment, Supervision (2)

Instructional Guidance
Assign specific objectives to be covered during CTT time in KEP-GP-43 and KEP-ST VI. Emphasize the various components and the functions they perform in each of the five oscillator types. Insure that each student can identify the type of oscillator by employing this component function approach. Analyze the effects of oscillator loading and show methods of compensation. Introduce the laboratory exercise and briefly discuss special procedures and desired outcomes.

PLAN OF INSTRUCTION/LESSON PLAN PART I

NAME OF INSTRUCTOR	COURSE TITLE
	Electronic Principles

BLOCK NUMBER	BLOCK TITLE
VI	Solid State Wave Generating and Wave Shaping Circuits

1 COURSE CONTENT	2 DURATION (Hours)
3. Solid State RC Oscillators (Module 44)	5 (4/1)

a. From a schematic diagram of any one of the following oscillators, select the component(s) that comprise the feedback loop(s), frequency determining device, forward bias network, amplitude adjustment, and the frequency adjustment: Phase Shift; Wien Bridge. CTS: 5f(2) Meas: W

(1) Phase Shift

(a) Purpose of each component.

(b) Explain operation in terms of

1 regenerative feedback path.

2 regenerative feedback amplitude.

3 frequency determining device.

4 tuning.

(c) Explain the need for a total phase shift of 180 degrees through the RC network.

(d) Explain the resulting amplitude changes through each phase shift network.

(2) Wien Bridge

(a) Purpose of each component.

(b) Explain operation in terms of

1 regenerative feedback path.

SUPERVISOR APPROVAL OF LESSON PLAN (PART II)

SIGNATURE	DATE	SIGNATURE	DATE

PLAN OF INSTRUCTION NO.	DATE	PAGE NO.
3AQR30020-1	20 November 1975	53

12

2 regenerative feedback amplitude.

3 degenerative feedback path.

4 degenerative feedback amplitude.

5 frequency determining device.

6 tuning.

(c) Describe the phase shifts that result from the series and parallel RC networks.

(d) Show the effect of changing both capacitors or resistors on the operating frequency.

b. Given a trainer and oscilloscope measure and calculate the phase shift in degrees of each RC network of an RC oscillator within ± 10 percent accuracy. CTS: 2a, 5f(2) Meas: PC

(1) Review the use of the oscilloscope.

SUPPORT MATERIALS AND GUIDANCE

Student Instructional Materials
KEP-GP-44, Solid State RC Oscillators
KEP-ST-VI
KEP-110

Audio Visual Aids
TVK 30-517, Wein Bridge Oscillator (Transistorized)

Training Equipment
Phase Shift Oscillator Trainer 5016 (1)
Oscilloscope (1)
Multimeter (1)
Transistor Power Supply 4649 (1)

Training Methods
Discussion (3 hrs) and/or Programmed Self Instruction
Performance (1 hr)
CTT Assignment (1 hr)

Multiple Instructor Requirements
Safety, Equipment, Supervision (2)

Instructional Guidance
Assign specific objectives to be covered during CTT time in KEP-GP-44. Use the same approach with the Phase shift and Wein bridge oscillators as recommended in module 43 objective a. Vectorially analyze phase shifting networks.

21

13

PLAN OF INSTRUCTION/LESSON PLAN PART I

NAME OF INSTRUCTOR	COURSE TITLE Electronic Principles

BLOCK NUMBER VI	BLOCK TITLE Solid State Wave Generating and Wave Shaping Circuits

1 COURSE CONTENT	2 DURATION (Hours)
4. Solid State Frequency Multipliers (Module 45)	4 (3/1)

a. Given a schematic diagram of a frequency multiplier, (with component values given)and the input frequency to the frequency multiplier, determine its output frequency and the factor by which its input frequency will be multiplied in the output. CTS: 5g(3) Meas: W

(1) Explain operation to include

- (a) harmonic generation.
- (b) frequency selection.
- (c) buffer action.

SUPERVISOR APPROVAL OF LESSON PLAN (PART II)

SIGNATURE	DATE	SIGNATURE	DATE

PLAN OF INSTRUCTION NO. 3AQR30020-1	DATE 20 November 1975	PAGE NO. 55

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SUPPORT MATERIALS AND GUIDANCE

Student Instructional Materials
KEP-GP-45, Solid State Frequency Multipliers
KEP-ST-VI
KEP-110

Training Methods
Discussion (3 hrs) and/or Programmed Self Instruction
CTT Assignment (1 hr)

Instructional Guidance
Make specific objective assignments to be completed during CTT time. Identify these objective areas in KEP-GP-45. Introduce this module with a discussion of harmonic generation. Show how these harmonics are effectively used and point out the restrictions.

15

PLAN OF INSTRUCTION/LESSON PLAN PART I

NAME OF INSTRUCTOR	COURSE TITLE Electronic Principles
BLOCK NUMBER VI	BLOCK TITLE Solid State Wave Generating and Wave Shaping Circuits

1 COURSE CONTENT	2 DURATION (Hours)
5. Solid State Pulsed and Blocking Oscillators (Module 46)	8 (6/2)
a. Given a collector loaded pulsed oscillator schematic diagram with an input gate and a group of waveforms, select the output. CTS: 5g(1) Meas: W	(2)
(1) Identify the schematic diagram of a collector-loaded pulsed oscillator.	
(2) Explain operation in terms of	
(a) flywheel effect.	
(b) gating on and off.	
(c) no regenerative feedback.	
(3) Relate the factors that determine the	
(a) time allowed for oscillations.	
(b) frequency of oscillations.	
(4) Explain damping of the output in terms of	
(a) Q of the tank circuit.	
(b) load on the tank.	
b. From a schematic diagram of a blocking oscillator, select the component(s) that primarily determine output signal pulse width; that determine output signal pulse recurrence time; that determine transistor cutoff time; that provide forward bias for the transistor. CTS: 5g(2) Meas: W	(1.5)

SUPERVISOR APPROVAL OF LESSON PLAN (PART II)

SIGNATURE	DATE	SIGNATURE	DATE

PLAN OF INSTRUCTION NO.	DATE	PAGE NO.
3AQR30020-1	20 November 1975	57

ATC FORM 133 APR 75 ATC Keesler 6-1029 REPLACES ATC FORMS 337, MAR 73, AND 770, AUG 72, WHICH WILL BE USED.

(1) Explain the start of capacitor discharge.

(2) Show relationship between the RC time constant and rest or cutoff time of the transistor.

c. Given the schematic diagram of a blocking oscillator and descriptive statements and waveforms, match the waveform to the statement. CTS: 5g(2) Meas: W (1.5)

(1) Identify the waveforms at the

(a) base.

(b) collector.

(c) output.

(2) Select the waveform that represents

(a) critical damping.

(b) under damping.

(c) over damping.

d. Given a schematic diagram of a synchronized blocking oscillator and a group of waveforms, select the ideal waveform that would be present in the feedback loop and in the output circuit. CTS: 5g(2) Meas: W (1)

(1) Explain the effect of triggering on PRT, PRF and frequency stability.

(2) Recognize the importance of sufficient trigger amplitude.

(3) Explain the operation of synchronized blocking oscillators as frequency dividers.

6. Measurement and Critique (Part 1 of 2 parts) 1

a. Measurement test

b. Test critique

SUPPORT MATERIALS AND GUIDANCE

Student Instructional Materials
KEP-GP-46, Solid State Pulsed and Blocking Oscillators
KEP-ST-VI
KEP-110

17

PLAN OF INSTRUCTION/LESSON PLAN PART I (Continuation Sheet)

COURSE CONTENT

Training Methods
Discussion (6 hrs) and/or Programmed Self Instruction
CTT Assignments (2 hrs)

Instructional Guidance
Make CTT assignments in KEP-GP-46, and Student Text VI. In order to effectively cover objective a, it will be necessary to discuss static conditions, input/output characteristics, and dynamic operation of the pulsed oscillator. The remaining objectives deal with blocking oscillators. Stress waveshapes and how they are changed by altering circuit parameters. Inform students that Part 1 of the measurement test covers modules 42 through 46.

PLAN OF INSTRUCTION NO.	DATE	PAGE NO.
3AQR30020-1	20 November 1975	59

18

PLAN OF INSTRUCTION/LESSON PLAN PART I

NAME OF INSTRUCTOR	COURSE TITLE Electronic Principles

BLOCK NUMBER VI	BLOCK TITLE Solid State Wave Generating and Wave Shaping Circuits

1 COURSE CONTENT	2 DURATION (Hours)

7. Solid State Multivibrators (Module 47) — 12 (9/3)

a. Given schematic diagrams of the following solid state multivibrators, select the name and primary use of each astable; each monostable; each bistable. CTS: 51(1) Meas: W — (1)

(1) Astable

(a) Identify schematic diagram.

(b) Explain the purpose of each component.

(c) Trace feedback path.

(d) Explain operation in terms of

1 regenerative feedback path.

2 cutoff and saturation.

(e) Given the schematic diagram of an astable multivibrator, identify the waveform at the base and collector of each transistor.

(2) Monostable

(a) Identify the schematic diagram.

(b) Explain the purpose of each component.

(c) Explain operation in terms of

1 stable condition.

2 need for triggers.

SUPERVISOR APPROVAL OF LESSON PLAN (PART II)

SIGNATURE	DATE	SIGNATURE	DATE

PLAN OF INSTRUCTION NO.	DATE	PAGE NO.
3AQR30020-1	20 November 1975	61

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3 regenerative feedback.

(d) Given the schematic diagram, identify the transistor that is conducting in the stable condition.

(e) Given the schematic diagram, identify the waveform at the base and collector of each transistor.

(3) Bistable

(a) Identify the schematic diagram.

(b) Explain the purpose of each component.

(c) Explain operation in terms of

1 two stable conditions.

2 need for triggers.

3 regenerative feedback.

(d) Given a schematic diagram, identify the waveform at the base and collector of each transistor.

(e) Compare the output frequency to the input trigger frequency.

(f) Identify the location of high frequency compensation capacitors.

(g) Given a drawing of several cycles of a square or rectangular wave, identify

1 rise time.

2 fall time.

3 pulse width.

4 rest time.

5 Pulse Recurrence Frequency.

6 Pulse Recurrence Time.

(h) Given a drawing of a square or rectangular wave, identify the transient interval.

b. Given the schematic diagram of a multivibrator and a list of statements, select the statement that describes the effects of time constants on pulse width, pulse recurrence frequency, (2.5) and pulse recurrence time. CTS: 5i(1) Meas: W

c. Given the schematic diagram of a multivibrator and a list of statements, select the statement that describes the effects of triggering on circuit operation. CTS: 5i(1) Meas: W (1)

d. Given a trainer with a malfunctioning multivibrator circuit, a schematic diagram, multimeter, and oscilloscope, determine the faulty component two out of three times. CTS: 5i(1) Meas: PC (3)

e. Given a schematic diagram of a Schmitt trigger and a list of symptoms, identify the faulty component. CTS: 5i(4) Meas: W (1.5)

(1) Identify the schematic diagram.

(2) Purpose of each component

(3) Explain operation in terms of

(a) input and output waveforms.

(b) regenerative feedback circuit.

(4) Identify high frequency compensating capacitor.

SUPPORT MATERIALS AND GUIDANCE

Student Instructional Materials
KEP-GP-47, Solid State Multivibrators
KEP-ST-VI
KEP-110
KEP-PT-47, Solid State Multivibrators

Audio Visual Aids
TVK 30-811, Monostable Multivibrator (Transistorized)

Training Equipment
Sweep Generator Trainer 5932 (1)
Transistor Power Supply 4649 (1)
Oscilloscope (1)
Multimeter (1)

Training Methods
Discussion (6 hrs) and/or Programmed Self Instruction
Performance (3 hrs)
CTT Assignments (3 hrs)

PLAN OF INSTRUCTION/LESSON PLAN PART I (Continuation Sheet)

COURSE CONTENT

Multiple Instructor Requirements
Safety, Equipment, Supervision (2)

Instructional Guidance
Make specific objectives assignments to be completed during CTT time in KEP-GP-47. The programmed text should be recommended to students who experience difficulty in this module. Each type of multivibrator is analysed in terms of component composition, circuit variables and output waveshapes. Due to the inherent similarities of these multivibrators, it is important to maintain correct circuit to characteristics association. In order to facilitate troubleshooting multivibrators, recall the collector voltage levels at saturation (near 0V) and cutoff (V_{CC}). Introduce the laboratory exercise, and briefly discuss the procedures prior to assigning students to the trainers.

PLAN OF INSTRUCTION/LESSON PLAN PART I

NAME OF INSTRUCTOR	COURSE TITLE
	Electronic Principles

BLOCK NUMBER	BLOCK TITLE
VI	Solid State Wave Generating and Wave Shaping Circuits

1 COURSE CONTENT	2 DURATION (Hours)
8. Solid State Sawtooth Generators (Module 48)	8 (6/2)
a. Given the schematic diagram of a sawtooth generator and a list of statements, select the statement that describes the effects on output linearity when time constants, applied voltage, and input gate duration are changed. CTS: 5b(2), 5i(2) Meas: W	(3.5)

(1) Unijunction Sawtooth Generator

(a) Identify the schematic diagram.

(b) Purpose of each component

(c) Explain operation in terms of

1 on-off switch.

2 10% charge of capacitor.

(d) Given a schematic diagram, identify the capacitor's charge path and discharge path.

(e) Given a schematic diagram, identify the waveforms at the emitter and base one.

(f) Relate electrical length of sawtooth waveform to time.

(g) Relate physical length of sawtooth waveform to amplitude.

(h) Relate frequency stability to input triggers.

(i) Explain why input triggers can be applied to the emitter circuit or base two circuit.

SUPERVISOR APPROVAL OF LESSON PLAN (PART II)

SIGNATURE	DATE	SIGNATURE	DATE

PLAN OF INSTRUCTION NO.	DATE	PAGE NO.
3AQR30020-1	20 November 1975	65

ATC FORM APR 75 133 ATC Keesler 6-1020 REPLACES ATC FORMS 337, MAR 73, AND 770, AUG 72, WHICH WILL BE USED.

(j) Explain the effects of triggers on linearity.

(k) Relate linearity to emitter source voltage.

(2) Transistor Sawtooth Generator

(a) Identify the schematic diagram.

(b) Purpose of each component

(c) Explain operation in terms of

1 gating on and off.

2 10% charge of capacitor.

(d) Relate rise time to the duration of the input gate.

(e) Relate sawtooth linearity to R and C.

b. Given a trainer having a semiconductor sawtooth generator circuit, multimeter, and oscilloscope, measure the output amplitude and rise time within ± 10 percent accuracy. CTS: 5i(2) Meas: PC (1)

(1) Review the use of the oscilloscope and multimeter.

c. Given a trainer with a malfunctioning sawtooth generator circuit, a schematic diagram, multimeter, and oscilloscope, determine the faulty component two out of three times. CTS: 5i(2) Meas: PC (1.5)

SUPPORT MATERIALS AND GUIDANCE

Student Instructional Materials
KEP-GP-48, Solid State Sawtooth Generators
KEP-ST-VI
KEP-110

Audio Visual Aids
TVK 30-817, Unijunction Sawtooth Generator

Training Equipment
Sweep Generator Trainer 5932 (1)
Oscilloscope (1)
Multimeter (1)
Transistor Power Supply 4649 (1)

Training Methods
Discussion (3.5 hrs) and/or Programmed Self Instruction
Performance (2.5 hrs)
CTT Assignments (2 hrs)

PLAN OF INSTRUCTION/LESSON PLAN PART I (Continuation Sheet)

COURSE CONTENT

Multiple Instructor Requirements
Safety, Equipment, Supervision (2)

Instructional Guidance
Give students specific objectives to cover during CTT time in KEP-GP-48. Analyze a sawtooth waveshape from the standpoint of amplitude, duration and linearity. Show the relationship of these wave characteristics to the various components and overall operation of the sawtooth generator circuit. Introduce the two laboratory exercises. Stress safety, adherence to instructions, and logical troubleshooting techniques.

PLAN OF INSTRUCTION NO.	DATE	PAGE NO.
3AQR30020-1	20 November 1975	67

PLAN OF INSTRUCTION/LESSON PLAN PART I

NAME OF INSTRUCTOR	COURSE TITLE
	Electronic Principles

BLOCK NUMBER	BLOCK TITLE
VI	Solid State Wave Generating and Wave Shaping Circuits

1 COURSE CONTENT	2 DURATION (Hours)
9. Solid State Trapezoidal Generators (Module 49)	7 (5/2)

a. Given the schematic diagram of a trapezoidal wave generator and a list of statements, select the statement that describes the effects on output linearity when time constants, applied voltage, and input gate duration are changed. CTS: 5i(3) Meas: W

(1) Identify the schematic diagram.

(2) Purpose of each component

(3) Given a trapezoidal waveform, identify the

(a) jump voltage.

(b) slope (rise time) voltage.

(c) fall time voltage.

(4) Describe the effects on linearity and jump voltage when resistor values are changed.

b. Given a trainer having a semiconductor trapezoidal wave generator circuit, multimeter, and oscilloscope, measure the output amplitude, rise time, and jump voltage within ±10 percent accuracy. CTS : 5i(3) Meas: PC

c. Given a trainer with a malfunctioning trapezoidal wave generator circuit, a schematic diagram, multimeter, and oscilloscope determine the faulty component two out of three times. CTS: 5i(3) Meas: PC

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SIGNATURE	DATE	SIGNATURE	DATE

PLAN OF INSTRUCTION NO.	DATE	PAGE NO.
3AQR30020-1 [illegible]	20 November 1975	69

ATC FORM APR 75 133 ATC Keesler 6-1029 REPLACES ATC FORMS 337, MAR 73, AND 770, AUG 72, WHICH WILL BE USED.

SUPPORT MATERIALS AND GUIDANCE

Student Instructional Materials
KEP-GP-49, Solid State Trapezoidal Generators
KEP-ST-VI
KEP-110
KEP-PT-49, Solid State Trapezoidal Generators

Training Equipment
Sweep Generator Trainer 5932 (1)
Oscilloscope (1)
Transistor Power Supply 4649 (1)
Multimeter (1)

Training Methods
Discussion (4 hrs) and/or Programmed Self Instruction
Performance (1 hr)
CTT Assignments (2 hrs)

Multiple Instructor Requirements
Safety, Equipment, Supervision (2)

Instructional Guidance
Assign specific objectives to be covered during CTT time in KEP-GP-49. Recall the waveform analysis discussed in module 48, and show how it is related to the trapezoidal wave. Analyze the circuit operation and discuss the effects that certain components have on the output. Introduce and briefly discuss the two laboratory exercises to be performed.

27

PLAN OF INSTRUCTION/LESSON PLAN PART I

NAME OF INSTRUCTOR	COURSE TITLE Electronic Principles

BLOCK NUMBER VI	BLOCK TITLE Solid State Wave Generating and Wave Shaping Circuits

1 COURSE CONTENT	2 DURATION (Hours)
10. Solid State Limiters and Clampers (Module 50)	11 (9/2)
a. Given the input waveform to the following solid state diode limiters and a group of output waveforms, select the waveform that would be present at the output of the named diode limiter: Series positive; Series negative; Shunt negative with bias; Shunt positive with bias. CTS: 5e Meas: W	(2)

(1) Purpose of a limiter

(2) Series positive

(a) Identify the schematic diagram.

(b) Explain operation in terms of a voltage divider.

(c) Given an input signal and schematic diagram, identify the output waveform.

(3) Series negative

(a) Identify the schematic diagram.

(b) Explain operation in terms of a voltage divider.

(c) Given an input signal and schematic diagram, identify the output waveform.

(4) Shunt limiters (positive and negative)

(a) Identify the schematic diagram.

(b) Explain operation in terms of a voltage divider.

(c) Given an input signal and a schematic diagram, identify the output waveform.

SUPERVISOR APPROVAL OF LESSON PLAN (PART II)

SIGNATURE	DATE	SIGNATURE	DATE

PLAN OF INSTRUCTION NO.	DATE	PAGE NO.
3AQR30020-1	20 November 1975	71

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(5) Biased Shunt limiters (positive and negative)

(a) Identify the schematic diagram.

(b) Explain operation in terms of a voltage divider.

(c) Given an input signal amplitude, the schematic diagram, and the amount and polarity of bias, identify the output signal.

(d) Identify the schematic diagram of a double diode limiter.

b. Given schematic diagrams of biased diode shunt limiters and a list of statements, select the statement that describes the effect on limiting when bias is changed. CTS: 5e Meas: W (1)

c. Given the input waveform to a zener diode limiter, a specified breakdown voltage, and a group of output waveforms, select the waveform that would be present at the output. CTS: 5b(7), 5e Meas: W (1)

(1) Explain the relationship between breakdown voltage and limiting.

d. Given the schematic diagram of a transistor limiter and a list of statements, select the statement that describes the effect on limiting when bias is changed. CTS: 5e Meas: W (2)

(1) Explain operation in terms of

(a) operating point.

(b) input amplitude.

(c) saturation and/or cutoff.

(2) Relate collector voltage levels to saturation and cutoff limiting.

e. Given the input waveform to the following solid state diode clampers and a group of output waveforms, select the waveform that would be present at the output of the named diode clamper: Negative with bias; Positive with bias. CTS: 5e Meas: W (1.5)

(1) Negative with bias and positive with bias

(a) Purpose of clamper

(b) Identify the schematic diagram.

(c) Explain operation in terms of

1 input and output signal references.

2 time constants.

COURSE CONTENT

f. Given a trainer having components for a diode limiter, connect the components as a series positive and/or negative limiter. CTS: 5e Meas: PC (.5)

g. Given a trainer having components for a diode limiter, an oscilloscope and a multimeter, connect the components as a shunt limiter with bias and determine the effects of limiting when bias is changed. CTS: 5e Meas: PC (.5)

h. Given a trainer having components for a diode clamper, an oscilloscope and a multimeter, connect the components as a negative or positive clamper with bias and determine the effects on the voltage reference of the clamper output when bias is changed. CTS: 5e Meas: PC (.5)

11. Related Training (identified in course chart) 2

12. Measurement and Critique (Part 2 of 2 parts) 1

a. Measurement test

b. Test critique

SUPPORT MATERIALS AND GUIDANCE

Student Instructional Materials
KEP-GP-50, Solid State Limiters and Clampers
KEP-ST-VI
KEP-110

Audio Visual Aids
TVK 30-504, Triode Limiters
TVK 30-505, Duo-Diode Limiter (TSTR)

Training Equipment
Limiters and Clampers Trainer 5925 (1)
Oscilloscope (1)
Multimeter (1)

Training Methods
Discussion (7.5 hrs) and/or Programmed Self Instruction
Performance (1.5 hrs)
CTT Assignments (2 hrs)

Multiple Instructor Requirements
Safety, Equipment, Supervision (2)

Instructional Guidance

Make specific objective assignments to be completed during CTT time in KEP-GP-50. Discuss the basic principles and functions of limiting circuits. Insure that each student can identify the type of limiter, bias consideration and its effect on the input waveshape. Use the same approach for clamping circuits. Have the class briefly scan through the laboratory exercises, discuss any special techniques and assign students to lab positions. Inform students that Part 2 of the measurement test covers modules 47 through 50.

31

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Prepared by Keesler TTC
KEP-ST-VI

Technical Training

Electronic Principles

Volume VI

SOLID STATE WAVE GENERATING AND WAVE SHAPING CIRCUITS

July 1974

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Electronic Principles Department
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KEP-ST-VI
July 1974

Electronic Principles

Block VI

SOLID STATE WAVE GENERATING AND WAVE SHAPING CIRCUITS

This Student Text is the prime source of information for achieving the objectives of this block. This publication is designed for training purposes only and should not be used as a basis for job performance in the field.

CONTENTS

CHAPTER	TITLE	PAGE
1	Principles of Wave Generation	1-1
2	Sine-Wave Oscillators	2-1
3	Pulsed Oscillators	3-1
4	Blocking Oscillators	4-1
5	Multivibrators	5-1
6	Time Base Generators	6-1
7	Limiters and Clampers	7-1

Errata for Student Text KEP-ST-VI, Dated July 1974 15 April 1975

PAGE	PARA	LINE	CORRECTION
2-2	2-10	5	Change formula to read $fr = \dfrac{.159}{\sqrt{LC}}$
2-14	2-103	3	Change formula to read $F_o = \dfrac{1}{2\pi \sqrt{(R1)(R2)(C2)(C1)}}$
4-3	4-15	last	Change "R1" to "RL".
4-5	4-23	4	Change figure number to 4-7B.
5-2	Figure 5-3		Change label "TRANSIENT INTERNAL" to "TRANSIENT INTERVAL"
5-3	5-11	7	Change "19.2" to "9.6"
5-6	Figure 5-10		Label components as indicated in figure 1 of this Errata.
5-7	5-38	4	Change "R2" to "R3"
5-8	Figure 5-13		Use figure 2 of this Errata in place of figure 5-13.

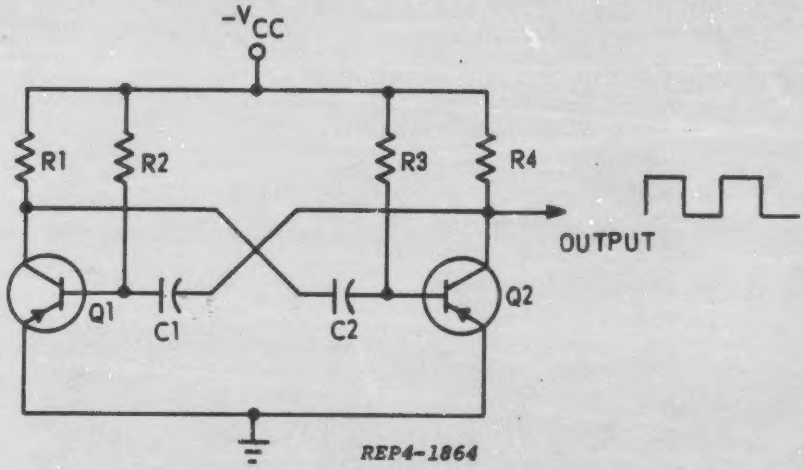

Figure 1. Astable Multivibrator (PNP)

PAGE	PARA	LINE	CORRECTION
5-12	5-71	2nd to last	Change paragraph "5-67" to "5-68".
6-7	6-29	4	Change figure number from "6-5" to "6-9".
6-8	Figure 6-10		Change figure number from "6-10" to "6-11".
7-9	7-44	4	Change "CR2" to "CR1".
7-11	7-60	9	Omit the sentence beginning "From point 2 to point . . . ."
7-16	Figure 7-23		Invert the signal shown to the right of the load line. Relabel it as shown in figure 3 and add "(BASE CURRENT)" to the words "INPUT SIGNAL".

PAGE	PARA	LINE	CORRECTION
7-19	7-82	9	Change figure number to "7-26A."
7-24	7-120	1	Change "T," to "T2,".

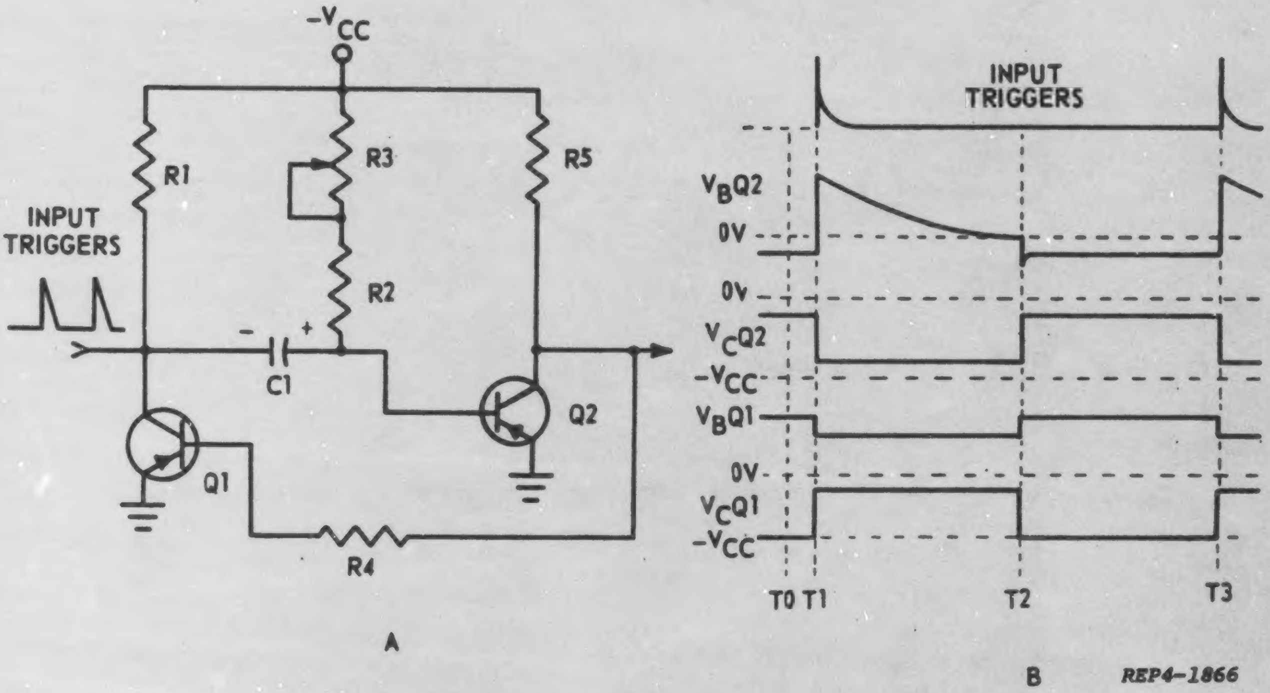
-VCC
R1
R3
R5
R2
INPUT TRIGGERS
C1
Q1
Q2
R4
A
INPUT TRIGGERS
VBQ2
0V
0V
VCQ2
-VCC
VBQ1
0V
VCQ1
-VCC
T0
T1
T2
T3
B
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Figure 2. Monostable Multivibrator with Waveshapes.

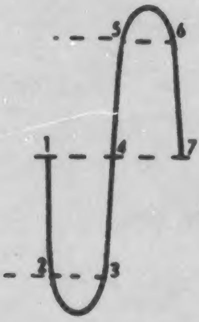

Figure 3.

Chapter 1

PRINCIPLES OF WAVE GENERATION

1-1. Wave generators play a prominent role in the field of electronics. They generate signals from a few hertz to several gigahertz (10^9). Modern wave generators use many different circuits capable of generating such outputs as sinusiodal, square, rectangular, sawtooth, or trapezoidal waveshapes.

1-2. One type of wave generator is called an oscillator. An oscillator is generally free-running and can be regarded as an amplifier which provides its own signal input. The study of oscillators, therefore, naturally follows a study of amplifiers. In this chapter, we classify oscillators as to waveshape and establish requirements for continuous oscillation. The most common types of wave generators and their output waveforms are discussed.

1-3. Classification

1-4. Wave generators can be classified, according to their output waveshapes, into two broad categories: sinusoidal and nonsinusoidal oscillators.

1-5. A sinusoidal oscillator produces a sine-wave output signal. Ideally, the output is a pure sine wave of constant peak amplitude with no variation in frequency. Actually, something less than this is obtainable. The degree to which the ideal is approached depends upon such related factors as class of operation, transistor characteristics, frequency stability, and amplitude stability.

1-6. Sine wave generators can produce signals ranging from a low audio frequency to very high radio and microwave frequencies. Many low-frequency types use resistors and capacitors to form their frequency determining network and are, therefore, referred to as *RC* oscillators. They find wide application in the audio-frequency range.

1-7. Another type of sine wave generator uses inductors and capacitors for frequency determining networks; these are the LC type oscillators. Oscillators using tank circuits (LC types) are commonly used at radio frequencies; they are not popular for extremely low-frequency generation, because the inductors and capacitors become large, heavy, and costly.

1-8. A third type sinusiodal oscillator is the crystal-controlled oscillator. The crystal-controlled oscillator provides excellent frequency stability, and is used from the middle of the audio through the radio-frequency range.

1-9. Nonsinusiodal oscillators generate complex waveforms such as square, rectangular, trigger, or sawtooth. Because their outputs are generally characterized by a sudden change, or relaxation, the name "relaxation oscillator" is often applied to them. The signal frequency of these oscillators is usually governed by the charge and discharge of a capacitor in series with a resistor. Some types, however, contain inductors that affect the output frequency. Thus, like sinusoidal oscillators, both RC and LC arrangements are used for frequency determination. Within this category are multivibrators, blocking and pulsed oscillators, and sawtooth and trapezoidal generators.

1-10. A triggered or gated signal generator is essentially one of the sinusoidal or nonsinusoidal types which is biased so that it generates a signal only when a trigger or gate is applied from an external source.

1-11. Requirements

1-12. Now, we will discuss briefly the conditions required for oscillations and some desirable performance characteristics. What characteristics are most important? How can these characteristics be improved? Why choose one type over another for a particular job? We need to consider these questions before starting into the oscillator circuitry. The basic requirements for sustained oscillations are AMPLIFICATION, FEEDBACK, and a FREQUENCY DETERMINING DEVICE.

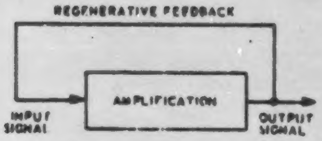

Figure 1-1. Basic Oscillator Block Diagram

1-13. An oscillator can be thought of as an amplifier that provides itself with a signal input. By definition, an oscillator is a device that converts DC power to AC power at a predetermined freqqency. The primary purpose of an oscillator, then, is to generate a given waveform at a constant peak amplitude and specific frequency and to maintain this waveform within certain limits.

1-14. Like an amplifier, an oscillator needs a power source for amplification. Since amplification of signal power occurs from input to output, it follows that a portion of the output can be fed back for use as the input, as shown in figure 1-1. Adequate power must be fed back to the input circuit for the oscillator to drive itself and be a signal generator. Not only must the feedback signal be strong enough but, to be self-driven, the feedback signal must be regenerative. With a regenerative signal, which has enough power to overcome the circuit losses, oscillations can be sustained.

1-15. A practical signal generator must oscillate at a predetermined frequency, so a frequency determining network is required. This is a form of filter which passes only the desired signal. With no frequency-determining network or device, the stage will oscillate in a random manner and the output frequency cannot be predicted.

1-16. From what has been said, we can review the requirements for an oscillator: first, amplification is required to provide the necessary gain for the signal; amplification implies a power source. Second, sufficient regenerative feedback is required to maintain a predetermined frequency.

1-17. Depending upon the application, requirements in addition to the basic ones may determine the type of oscillator chosen for use. Modification of associated circuitry may be necessary to achieve the performance required. Let's consider some factors that account for the complexity and diversity of oscillators.

1-18. Virtually every piece of equipment that uses an oscillator has two stability requirements: amplitude stability and frequency stability. Amplitude stability refers to the ability of the oscillator to maintain a constant amplitude output waveform. The less deviation from a predetermined amplitude, the better the amplitude stability. Frequency stability refers to the ability of the oscillator to maintain its operating frequency. The less the oscillator drifts from its operating frequency, the better the frequency stability. The degree to which these requirements must be met depends on the demands of the equipment.

1-19. To achieve a constant frequency and amplitude, extreme care must be taken to prevent variations in load, bias, and component characteristics. Load variations can have a marked effect on the stability of an oscillator's output. It is necessary, therefore, to minimize load changes.

1-20. Bias variations affect the operating point; this will alter the amplification and other circuit constants. A well-regulated power supply and bias stabilizing circuitry are required to insure a constant, uniform signal output.

1-21. Signal irregularities can also be caused by components which change in value or characteristics, as a result of environmental conditions.

1-22. Output power is another requirement that is dictated by the application. Generally speaking, high power is obtained at some sacrifice in stability. When both requirements are to be met, a low-power, stable oscillator can be followed by a high power "buffer" amplifier. The buffer provides isolation to prevent changes in load from affecting the oscillator.

1-23. If the oscillator stage must develop high output power, efficiency becomes important. Many oscillators are operated Class C to increase efficiency. Some types of oscillators cannot be operated Class C. Therefore, not all oscillators are suited for applications that require high power.

1-24. The frequency of the wanted signal also imposes certain requirements. If the frequency is high, a transistor must be selected that has low interelement capacitance. Special circuits make use of the interelement capacitances to obtain the desired frequency output.

1-25. Sine Wave Generators

1-26. We mentioned that RC networks, LC tanks, and crystals may appear in sine wave oscillator circuits. An ordinary amplifier can be made into a sine wave oscillator by providing regenerative feedback through an RC network. Figure 1-2A shows an amplifier with an RC network which provides both the regenerative feedback and the frequency determining device. Figure 1-2B shows a vector analysis of the signal at various points in the circuit.

1-27. Assume that the amplifier is a common emitter configuration, so the signal on the collector (A) is 180° out of phase with the signal on the base (D). To have regenerative feedback, the RC network must provide a 180° phase shift of the collector signal. When power is applied to the circuit, a noise voltage (noise contains many different frequencies) will appear on the collector. Vector A (figure 1-2B) represents the oscillator signal on the collector. As the signal couples through C1 and across R1, a phase shift occurs. The voltage across R1 (E_{R1}), represented by vector B, has been shifted in phase (about 60°) and reduced in amplitude. The signal at point B is then coupled to the next RC section (R2 and C2). By using the same size resistor and capacitor as before, another phase shift takes place. The signal at point C is the voltage across R2, represented by vector C. Now the signal at point C has been shifted about 120° and its amplitude is reduced still further. The same actions occur for the last section (R3 and C3). This signal experiences another phase shift, with further amplitude reduction. The signal at point D (E_{R3}) has been shifted 180° and is represented by vector D. You can see that a high gain amplifier must be used to provide adequate feedback power.

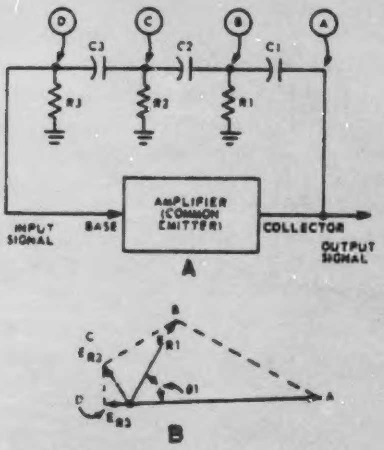

Figure 1-2. Vector Diagram of RC Oscillator

1-28. Notice that point D is the input to the base of the common emitter amplifier. Also, vector D shows that the signal on the base is regenerative or aiding the circuit operation. This is the regenerative feedback requirement. The 180° phase shift occurs only at one frequency. Exactly 60° shift per stage is not required, but the sum of the three phase shifts MUST equal 180°.

1-29. For a given RC network, only ONE frequency will be shifted exactly 180°. In other words, the network is frequency selective. You can appreciate this if you consider the fact that the lengths of vectors and their phase relationships depend on frequency ($X_C = \frac{1}{2\pi\sqrt{FC}}$). Therefore, the RC network is the frequency-determining device, since this vector construction is true for a single sine-wave signal. The frequency of oscillations is governed by the values of resistance and capacitance in these sections. Variable resistors and capacitors may be used to provide tuning in the feedback network. For a sine wave output, the amplifier is biased for Class A operation.

1-30. Some sine wave generators use resonant circuits (LC). You already know how a resonant circuit stores energy alternately in the inductor and capacitor; this produces an output which is a sine wave. You studied this action, known as the "fly-wheel effect," in parallel resonant circuits.

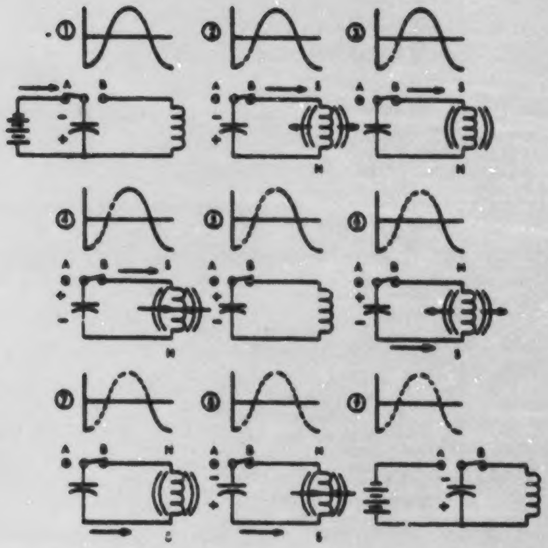

Figure 1-3. Flywheel Effect

1-31. Refer to figure 1-3, 1 through 9, and follow explanation to review the flywheel effect. Each numbered section has a circuit, and the resulting waveform represents the flywheel action.

1-32. With the switch in position A, figure 1-3-1, the capacitor charges quickly to the voltage of the battery. When the switch is placed in position B, the charged capacitor (which acts as a voltage source) begins to discharge through the inductance (which acts as a load). The current flows through the coil (as the capacitor discharges) and builds up a magnetic field around the coil, figure 1-3-2. In this way, the energy stored in the dielectric is converted into energy stored in the magnetic field. The arrows indicate the direction of electron flow and the motion of the magnetic field. When the number of electrons on both plates of the capacitor is equal, the capacitor is discharged. It is no longer a voltage source for current flow, figure 1-3-1. The broken lines tracing through the waveform represent the development of the oscillation.

1-33. When the capacitor is discharged, there is no force to maintain current flow and sustain the magnetic field. So, the magnetic field collapses, inducing a voltage which causes current to continue flowing in the same direction, charging the capacitor with the polarity shown, figure 1-3-4. Current continues until the magnetic field is completely collapsed and the capacitor is charged, figure 1-3-5. The output voltage of the tank circuit has a polarity which is now positive.

1-34. The capacitor begins to discharge again through the coil, figure 1-3-6. This time, however, the direction of the current flow is reversed, as indicated by the arrow. Again, the magnetic field expands as the capacitor discharges, decreasing the output voltage. This continues until the capacitor discharges, figure 1-3-7. At that instant, the magnetic field starts to collapse causing current to continue to flow in the same direction, charging the capacitor as shown in figure 1-3-8. When the capacitor is charged, the conditions in the tank circuit have returned to those that existed at the instant the switch was placed in position B. The entire process continues at a rate determined by the values of L and C. The output waveshape, figure 1-3-9, taken across the tank circuit is a sine wave which occurs as the inductor and the capacitor alternately store and release energy in their respective fields.

1-35. If there were no internal resistances in a tank circuit, oscillations would continue indefinitely (figure 1-4A). Each resonant circuit, however, contains some resistance which dissipates power. This power loss causes the amplitude to decrease as shown in figure 1-4 (B & C). The reduction of oscillation amplitude in an oscillator circuit is defined as "damping". Damping is caused by tank and load resistances. The larger the tank resistance, the greater the amount of damping. Loading the tank causes the same effect as increasing the task's internal resistance. The effect of tank damping in oscillators is overcome by applying regenerative feedback.

1-36. Figure 1-5 shows a block diagram for a typical LC oscillator. Observe the basic requirements for sustained oscillations: amplification, frequency determining device and regenerative feedback.

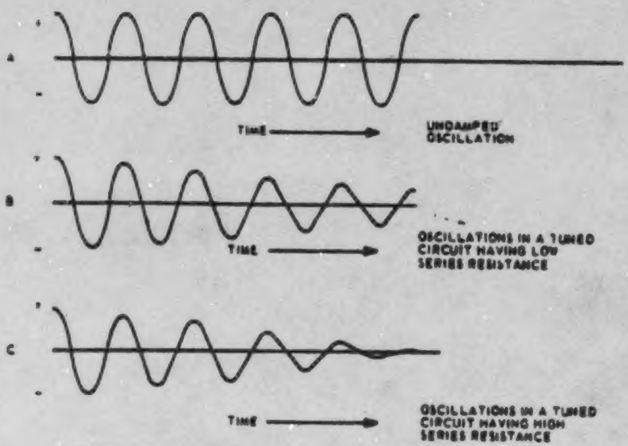

Figure 1-4. Effects of Damping

1-37. The amplifier supplies energy to begin the flywheel effect; the LC network provides initial oscillations, with its output returned to the amplifier through the regenerative feedback network to sustain oscillations. If the tank circuit has a high Q, the amplifier can be operated Class C. The LC components generate an output waveform that varies at a sinusoidal rate.

1-38. When a tank circuit is used to develop oscillations, the output frequency of the oscillator is primarily the resonant frequency of the tank circuit, and can be found by the formula: $f_o = \frac{1}{2\pi\sqrt{LC}}$. This formula is valid for tank circuits, used in oscillators, which have a Q greater than 10.

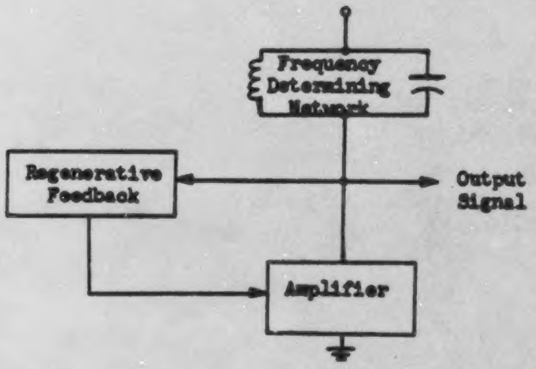

Figure 1-5. LC Oscillator Block Diagram

1-39. Another frequency determining device (FDD) is the crystal. The crystal may be used with a tank circuit, or it may perform alone.

1-40. Crystals exhibit a characteristic known as the "piezoelectric effect." The piezoelectric effect is the property of a crystal by which mechanical forces produce electrical charges, and conversely, electrical charges produce mechanical forces. This is a form of oscillation, like the flywheel effect of a tank circuit.

1-41. The piezoelectric effect is exhibited by a number of crystal substances. The most important of these is quartz. Although quartz exhibits the piezoelectric effect to a lesser degree than Rochelle salt, quartz is used for frequency control in oscillators because of its greater mechanical strength. Tourmaline is similar to quartz as it has high strength but it is more expensive. In this discussion, we will deal only with the quartz crystal.

1-42. The crystals used in oscillator circuits are thin sheets or wafers cut from natural or synthetic crystal and ground to a specific thickness to obtain the desired resonant frequency.

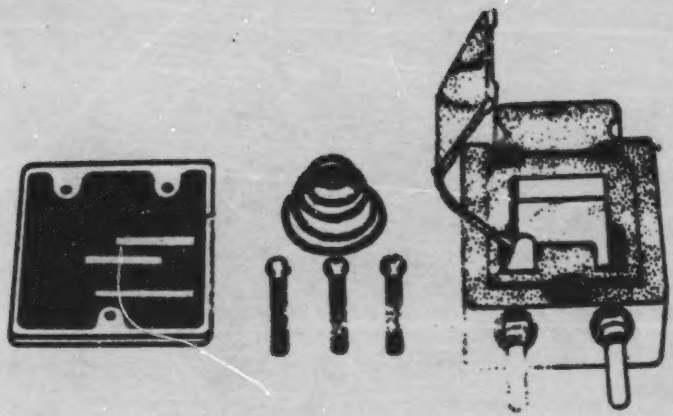

Figure 1-6. Crystal Holder

1-43. Crystals are mounted in holders, which support them physically and provide electrodes by which voltage is applied. The holder must allow the crystal freedom for vibration. There are many different types of holders. One type is shown in figure 1-6.

1-44. The frequency for which a crystal is ground is called the "natural resonant frequency" of the crystal. Voltage applied to the crystal produces mechanical vibrations which, in turn, produce a terminal voltage of the crystal's resonant frequency. The electrical circuit associated with a vibrating crystal can be represented by an equivalent circuit composed of capacitance, inductance, and resistance.

1-45. Figure 1-7A illustrates the symbol of a crystal. Figure 1-7B shows an equivalent circuit for the crystal, and figure 1-7C shows an equivalent circuit for the crystal, and the holder. C1 represents the capacitance between the metal plates of the holder.

1-46. Electrical circuits involving crystals can be analyzed by replacing the crystal with its equivalent network and then determining the behavior of the resulting circuit. This does NOT mean, however, that a coil and a capacitor can be substituted for the crystal to give the same electrical characteristics.

1-47. The Q of a crystal is many times greater than that of an LC tank circuit. The high Q is present because the resistance in the crystal is extremely small. Commercially-produced crystals range in Q from 5,000 to 30,000 indicating the reactance is five thousand to thirty thousand times the resistance. The high Q causes the

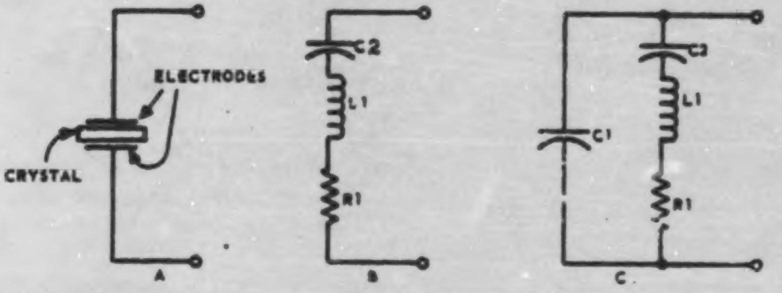

Figure 1-7. Crystal Symbols and Equivalent Circuits

41

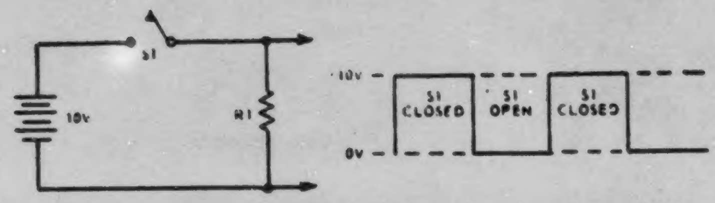

Figure 1-8. Square Waves

resonant circuit frequency stability to be much greater than that of an ordinary LC tank circuit. This is an important reason why a crystal is used in many sine wave generator circuits.

1-48. Square and Rectangular Wave Generators.

1-49. Nonsinusoidal wave generators (square, rectangular, sawtooth, and trapezoidal) use the principle of an on-off switch. As illustrated in figure 1-8, a square wave can be produced by connecting a resistance to a voltage source through a switch.

1-50. With the switch open, there is zero volts across R1. When the switch is closed, the voltage of the battery is applied across the resistor. If the switch is opened and closed for equal lengths of time, the output voltage will be a series of square waves. If the lengths of time are unequal the output will be a rectangular wave; see figure 1-9. The square or rectangular wave represents the two extremes to be reached. The switch allows current to flow easily for one time period; then it prevents current from flowing during the other time period.

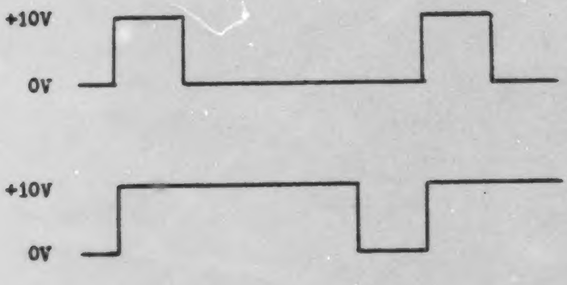

Figure 1-9. Rectangular Waves

1-51. The square wave contains a fundamental frequency and an infinite number of odd harmonics which have specific amplitude and phase relationships. The rectangular wave contains a fundamental and specific harmonically-related frequencies, determined by the time of each alternation.

1-52. Since nonsinusoidal waves contain many frequencies, the circuit generating these waves must have wide-band characteristics. That is, the frequency response of the generator and its associated circuitry must be sufficient to pass all the frequencies of the waveform without distortion.

1-53. Because a fundamental and harmonics are to be generated, there must be a nonlinear device. The nonlinear device is a transistor operated in the saturation and cutoff regions. Further, to sustain the circuit operation, regenerative feedback is required with amplitude large enough to sustain oscillations.

1-59. The frequency-determining device will be internal to the circuit if it is free-running, or external if a trigger or pulse is used to control frequency. Internal frequency control commonly uses time constant arrangements.

1-55. A basic block diagram of a square or rectangular wave generator is shown in figure 1-10. The block diagram is like that of a sine wave generator. The operation differs because of the amplitude of feedback. With

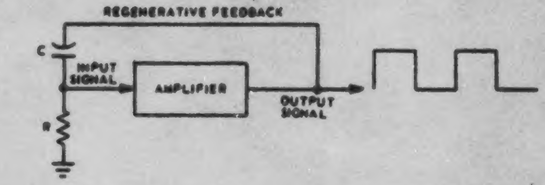

Figure 1-10. Square or Rectangular Wave Generator

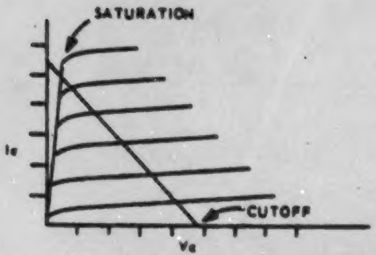

Figure 1-11. Nonsinusoidal Wave Generator Switching Method

PNP common base configuration amplifiers, as the output goes positive, a large regenerative feedback signal drives the amplifier into cutoff. The circuit stays in this condition until C charges to the output voltage. Then, the circuit reverts to the opposite condition, saturation. The RC network controls the time that the circuit is cut off. The output waveform is square if the time for cutoff and saturation is the same. The output wave is rectangular if the cutoff and saturation times are unequal.

1-56. One primary consideration of a square or rectangular wave generator is the switching action. Figure 1-11 illustrates a transistor load line and the two extremes of the circuit, cutoff and saturation. For switching action to occur, the transistor must go from cutoff to saturation (or vice versa) in a minimum amount of time. If the transistor could go from one extreme to the other in zero time, the sides of the wave would be exactly perpendicular to a reference line; one requirement for a perfect square or rectangular wave. This is not possible. The closer the transistor circuit approaches this condition, the better the waveshape.

1-57. Another nonsinusoidal wave is called a "sawtooth" waveform, figure 1-12. A sawtooth wave can be described as a linear increase in voltage with respect to time (T0 to T1) and a rapid decay of voltage (T1 to T2).

1-58. Possibly the best way to illustrate the need for a sawtooth wave is in an oscilloscope. The horizontal deflection of the beam is directly related to the voltage applied to the horizontal deflection plates. Therefore, to obtain a linear display on the oscilloscope, a linear voltage must be applied to the deflection plates.

1-59. The generation of a sawtooth wave uses on-off switching action, plus a characteristic of a capacitor. To illustrate the capacitor characteristic, refer to figure 1-13. Review the Universal Time Constant Chart which shows the relationship between the percentage of full charge and the time for charge. Sawtooth wave generators use the first 10 percent of full charge of a capacitor (lower left-hand corner of the chart). This first 10 percent of charge occurs in one-tenth of one time constant and gives the greatest amplitude change in the given time period. For example, during the second tenth of a time constant (between one-tenth and two-tenths TC), the amplitude change is 8 percent. As we progress further along the curve, the amplitude change becomes less for each time increment.

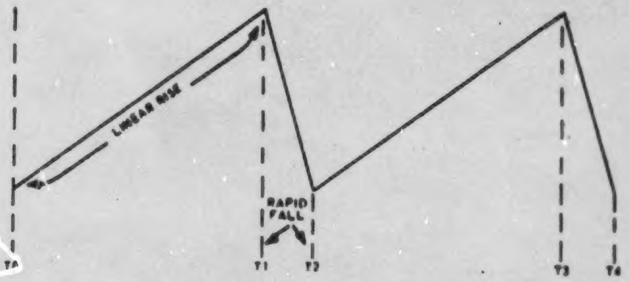

Figure 1-12. Sawtooth Waves

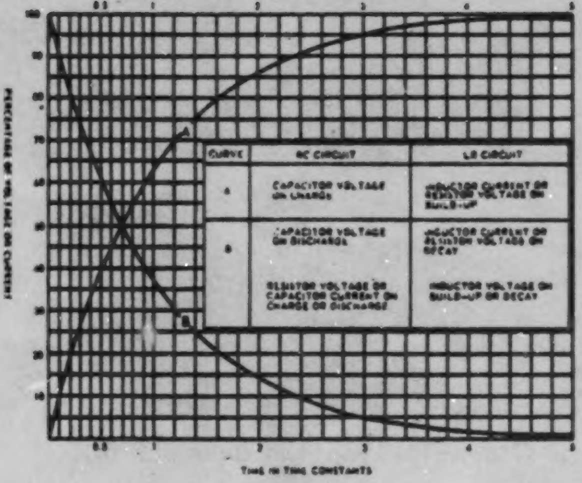

Figure 1-13. Universal Exponential Curves

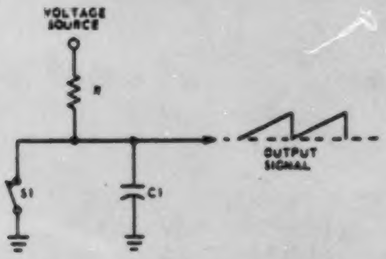

Figure 1-14. Sawtooth Generator Equivalent Circuit

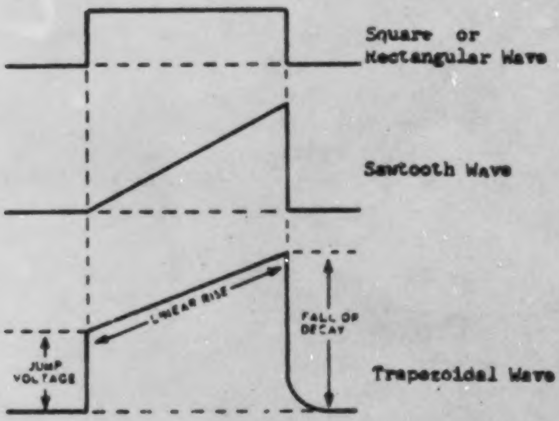

Figure 1-15. Trapezoidal Wave

1-60. Since a sawtooth wave generator normally uses only the first 10 percent of the capacitor's charge, when the wave reaches the 10 percent point the voltage is returned to zero. Refer to the simplified circuit shown in figure 1-14. With S1 closed, the capacitor is shorted out, and output voltage is zero. When S1 is opened, C starts charging through R toward the applied voltage. Since the output is taken across the capacitor, the voltage rises from zero volts as the capacitor charges. As soon as the capacitor has charged to 10 percent of the voltage applied, S1 is closed. The capacitor immediately discharges, and the output voltage returns to zero. Then the switch opens again, and the process repeats.

1-61. Most circuits use a transistor as the switch. When the transistor is biased near saturation, the voltage across the capacitor is nearly zero. When an applied gate cuts off the transistor, the capacitor starts charging toward V_{CC}. After 10 percent of the charge, the gate ends; this places forward bias on the transistor so the capacitor discharges, causing the voltage across the capacitor to drop rapidly toward zero.

1-62. A "trapezoidal" wave looks like a sawtooth wave on top of a square or rectangular wave (figure 1-15).

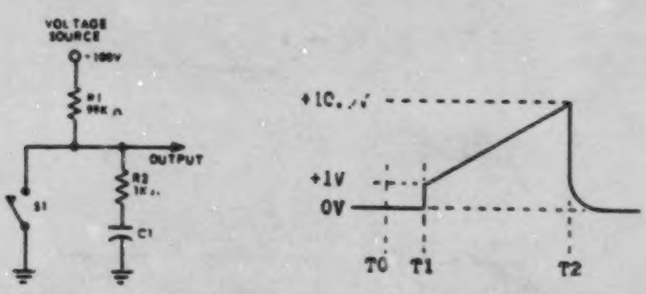

Figure 1-16. Trapezoidal Wave Generator Equivalent Circuit

1-63. The leading edge of a trapezoidal wave is called the ''jump'' voltage. The next portion is the linear rise of ''slope.'' The trailing edge is called the ''fall'' or ''decay''. A trapezoidal wave is used to furnish deflection current in the electromagnetic cathode ray tubes and is found in television and radar display systems. Electromagnetic CRTs use coils for the deflection system, and a linear rise in current is required. The square or rectangular wave portion provides the jump voltage for a linear rise in current through the resistance.

1-64. A simplified circuit of a trapezoidal wave generator is shown in figure 1-16.

1-65. Components R1, R2, and C1 connect from a power source to ground. One side of switch S1 is connected between R1 and R2, and the other side is connected to ground. To illustrate the operation, assume the following: E applied is 100 volts, R1 is 99 k ohms. With the switch closed at time T0, the output voltage is zero volts. At time T1, the switch is opened. At the first instant the capacitor acts as a short, so the circuit consists of a 99 k ohm resistor in series with a 1 k ohm resistor, and the voltage across R2 (the output voltage) immediately goes to plus 1 volt. This is how the jump voltage is derived.

1-66. The capacitor now begins to charge toward the applied voltage of 100 volts. To keep the sweep as linear as possible and get maximum change in voltage in minimum time, we use only the first 10 percent of full charge. Thus, the capacitor is allowed to charge from time T1 to T2, the capacitor has charged 10 volts; 90 volts across the two resistors drop the voltage across R2 to .9 volts. So, the output voltage at T2 is 10.9 volts. At time T2, the switch is again closed; the output goes to zero volts and the capacitor discharges through the switch and R2.

1-67. Sawtooth and trapezoidal wave generators are commonly called ''time base'' generators because the outputs are used to generate sweeps which are linear with respect to time.

Chapter 2

SINE-WAVE OSCILLATORS

2-1. As an electronics technician, you will spend many hours troubleshooting and repairing oscillator circuits. Oscillators are important circuits in communication systems, navigational aids, radar, and test equipment. The oscillator must generate a signal at a constant amplitude and frequency if the equipment is to function properly. This chapter covers the various types of sine-wave oscillators.

2-2. Have you ever been in an auditorium when the public address system developed a shrill whistle? This whistle is heard because the public address system becomes an oscillator. To understand how this whistle occurs, we will analyze a public address system. The system contains an amplifier, a microphone, and a loudspeaker as shown in Figure 2-1.

2-3. The whistle starts with a small noise picked up by the microphone. The noise is amplified by the amplifier and then sent to the speaker. With the microphone in the path of the speaker, the noise is fed back to the microphone which starts the process again. This continues until the amplifier is overdriven and the amplitude of the noise reaches a steady value. You hear this as a loud whistle. If you remove the microphone from the path of the speaker (break the feedback path), the oscillations will cease. Another method used to stop the oscillations is to decrease the gain of the amplifier. This will decrease the feedback amplitude to the point that oscillations cease.

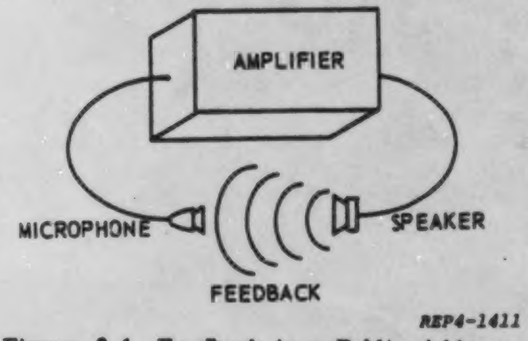

Figure 2-1. Feedback in a Public Address System

2-4. The basic requirements for sustained oscillations are (a) amplification, (b) a frequency determining device, and (c) regenerative feedback.

2-5. An amplifier and its associated circuitry requires a power source for its operation. Refer to Figure 2-2. The amplifier provides the necessary gain, and the feedback network provides regenerative feedback. The frequency determining device sets the output frequency.

2-6. Amplifier

2-7. The amplifier must provide enough gain for the output load and for regeneration, to maintain constant amplitude and frequency. The amplifier can be a common emitter, common collector, or common base configuration. The circuit is often a common emitter configuration because of its power gain characteristics, and because the input and output impedance can be matched easily.

2-8. Frequency Determining Device

2-9. The frequency determining device (FDD), as the name implies, determines the frequency of operation of the oscillator. Devices used include RC networks, LC tank circuits, and crystals.

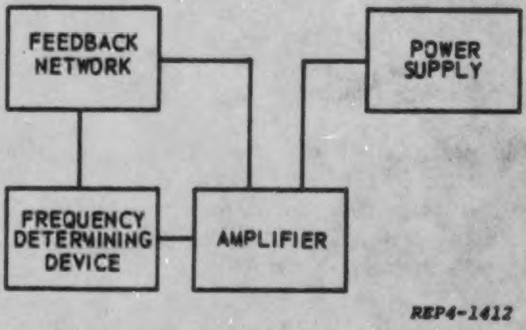

Figure 2-2. Block Diagram of an Oscillator

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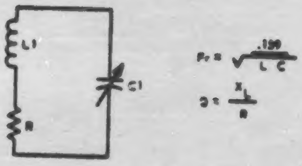
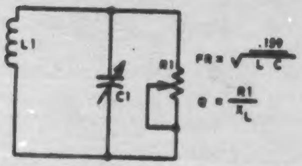


A. RESONANT CIRCUIT



B. RESONANT CIRCUIT WITH EXTERNAL LOADING

Figure 2-3. Tank Circuit Loading

2-10. A common FDD uses LC components in either series or parallel resonant circuits. The resonant frequency of a tank circuit is determined by the size of L and C, using the formula $f_r = \frac{.159}{LC}$. Changing tank capacitance or inductance will tune the tank. Decreasing C or L causes the resonant frequency of the tank to increase. Therefore, if either C or L is made larger, the resonant frequency of the tank circuit will decrease. By properly adjusting the capacitor or coil, the desired resonant frequency can be obtained.

2-11. Refer to Figure 2-3A. Resistor R represents the total internal resistance of the tank. Remember, R is one of the factors used to determine the Q of the tank, where the formula for Q is:

$$Q = \frac{X_L}{R} \text{ or } \frac{X_C}{R} \text{ when } X_L = X_C.$$

This formula shows that Q and internal resistance are inversely related. Assume that, at resonance, the ratio of reactance to resistance is greater than 20; the Q of the tank will be greater than 20.

2-12. Refer to Figure 2-3B and notice the external resistor R1. Resistor R1 can be used to control the Q of the tank. Q for this arrangement is $Q = \frac{R1}{X_L}$ (R in shunt).

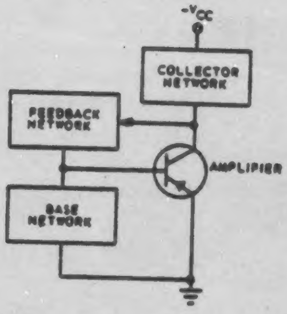


Figure 2-4. Oscillator Block Diagram

When R1 is made smaller (less resistance) the tank circuit is shunted with a low resistance which causes more losses in the circuit and, therefore, lowers the Q. This is a common method of changing the Q of a tank circuit. A limitation is the fact that the Q cannot be made any higher than it was before the resistor was added. All R1 can do is lower the Q.

2-13. When the FDD is a tank circuit, the L and C determine the frequency, but the Q of the tank determines the feedback requirement. A low Q requires more feedback than a high Q. The greater the feedback requirement, the greater the load on the complete oscillator circuit.

2-14. Regenerative Feedback

2-15. Feedback is the process of transferring energy from a high level point in a system to a low level point in a system. This usually means transferring energy from the output of an amplifier back to its input. If the feedback opposes the input signal, the feedback is degenerative. However, if the feedback aids the input signal, the feedback is regenerative.

2-16. Regenerative feedback is required in an oscillator. It furnishes the input signal to the amplifier. The amplified feedback signal offsets the damping in the FDD circuit. Since all circuits have some losses, the regenerative feedback must be equal to the losses and provide a circuit gain of unity.

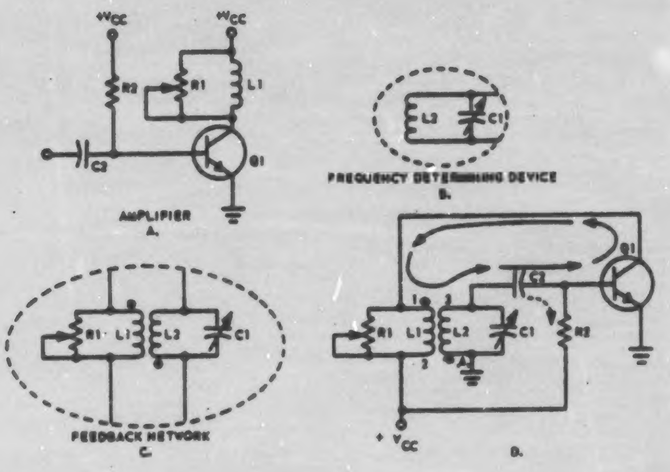


Figure 2-5. Oscillator Circuit

Unity gain means that circuit losses are being corrected.

2-17. Figure 2-4 shows a feedback network connected between the collector and base of a transistor amplifier. Since a common emitter configuration shifts the signal 180 degrees, the feedback network must shift the collector voltage an additional 180 degrees for it to be regenerative feedback. Transformers, resistance-capacitance networks, interelement capacitance, and inductance networks provide this 180-degree shift. With a common base or common collector amplifier configuration, no phase shift is required.

2-18. Armstrong Oscillator

2-19. We have discussed the requirements of oscillators. Let's put them together in a complete oscillator circuit.

2-20. Figure 2-5A shows a conventional amplifier. R2 provides the forward bias for Q1; C2 is a coupling capacitor; and L1 and R1 form the collector load impedance. This is a common emitter configuration which gives a 180-degree shift between the base and collector.

2-21. Figure 2-5B shows a frequency determining device composed of inductance L2 and capacitance C1. C1 is the tuning device used to adjust the resonant frequency to the desired value.

2-22. Figure 2-5C is the feedback network which uses collector load L1 as the primary and L2 as the secondary windings of a coupling transformer to provide 180-degree phase shift. Variable resistor R1 controls the amount of current through L1. With R1 adjusted for maximum resistance, most of the current flows through L1. The transformer now couples maximum signal into the tank circuit. This represents a large feedback amplitude. If R1 is adjusted for a smaller resistance, less current flows through L1, and less energy is coupled to the tank circuit, therefore, feedback amplitude decreases. R1 is adjusted so that the L1 current is adequate to sustain tank oscillation.

2-23. Figure 2-5D shows the complete oscillator circuit. By connecting the feedback network through coupling capacitor C2 to the base of Q1, we have a "closed loop" for feedback (shown by the solid arrows). Let's verify that the feedback is regenerative: assume a positive signal on the base of Q1. The transistor amplifies this signal and inverts it 180 degrees. The negative collector signal is applied to primary L1 of the transformer, which is connected so that there is a 180-degree phase shift between leads 1 and 3. The negative signal applied to lead 1 appears at lead 3 as a positive signal. The positive signal is now coupled through C2 to the base of Q1. Notice that we assumed a positive signal on the base, and the voltage fed back is of the same polarity. If we assume a negative signal voltage on the base, the feedback signal will be negative. In either case, the regenerative feedback offsets the damping in the FDD and has sufficient amplitude to provide a circuit gain of unity.

2-24. Figure 2-5D fulfills the requirements for an oscillator: amplification, a frequency determining device, and regenerative feedback. The schematic drawing is a "tuned base" oscillator, because the FDD is in the base unit. (If the FDD were in the collector circuit with C1 in parallel with L1, it would be a "tuned collector" oscillator.) This particular circuit is an Armstrong oscillator.

2-25. Refer to Figure 2-5D as we discuss the circuit operation. When V_{CC} is applied to the circuit, a small amount of base current flows through R2 which sets forward bias on Q1. This forward bias causes collector current to flow from ground through Q1 and L1 to $+V_{CC}$. The current through L1 develops a magnetic field which induces a voltage into the tank circuit. The voltage is positive at the top of L2 and C1. At this time, two actions occur: first, resonant tank-capacitor C1 charges to this voltage; the tank circuit now has stored energy. Second, coupling capacitor C2 couples the positive signal to the base of Q1. With a positive signal on its base, Q1 will conduct harder. With Q1 conducting harder, more current flows through L1, a larger voltage is induced into L2, and a larger positive signal is coupled back to the base of Q1. While this is taking place, the frequency determining device is storing more energy. C1 charges to the voltage induced into L2.

2-26. The transistor will continue to increase in conduction until it reaches saturation. At saturation, collector current of Q1 is at a maximum value and cannot increase any further. With a steady current through L1, the magnetic fields are not moving and no voltage is induced into the secondary.

2-27. With no external voltage applied, C1 now acts as a voltage source and discharges. As it does, it transfers its energy into the magnetic field of L2, and the voltage across C1 decreases. Now, let's look at C2.

2-28. The coupling capacitor has charged to approximately the same voltage as C1. As C1 discharges, C2 will discharge. The prime discharge path for C2 is through R2 (shown by the dashed arrow). As C2 discharges, the voltage drop across R2 reduces the forward bias on Q1, and collector current begins to decrease.

2-29. A decrease in collector current allows the magnetic field of L1 to collapse. The collapsing field of L1 now induces a negative voltage into the secondary which is coupled through C2 and makes the base of Q1 more negative. This, again, is regenerative action and it continues until Q1 is driven into cutoff.

2-30. When Q1 is cut off, the tank circuit continues to flywheel or oscillate. The flywheel effect not only produces a sine-wave signal, but it aids in keeping Q1 cut off. Without feedback, the oscillations of L2 and C1 would dampen out after several cycles. To insure that the amplitude of the signal remains constant, regenerative feedback is supplied to the tank once each cycle, as follows:

2-31. As the voltage across C1 reaches a maximum negative, C1 begins discharging toward zero volts. Q1 is still below cutoff. C1 continues to discharge through zero and becomes charged positively. The tank circuit voltage is coupled to the base of Q1, so the base voltage becomes positive and allows collector current to flow. The collector current causes a magnetic field in L1 which is coupled into the tank. The action replaces any lost energy in the tank circuit. This feedback also drives Q1 into saturation. After saturation is reached, the transistor is again driven into cutoff.

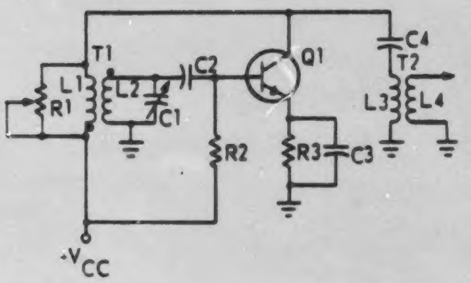


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Figure 2-6. Armstrong Oscillator

2-32. The operation of the Armstrong oscillator is basically this: power applied to the transistor allows energy to be applied to the tank circuit. When the transistor cuts off, the tank circuit oscillates. Once every cycle, the transistor conducts for a short period of time (Class C operation) and returns enough energy to the tank to insure a constant amplitude signal.

2-33. Class C operation has high efficiency and low loading characteristics. The longer Q1 is cut off, the less the loading on the frequency determining device.

2-34. For Class A operation, the feedback amplitude must be reduced, and C2 is usually larger. The reduced feedback amplitude prevents the amplifier from going all the way into saturation and cutoff, and the larger capacitor makes a longer time constant, so C2 cannot charge or discharge any appreciable amount.

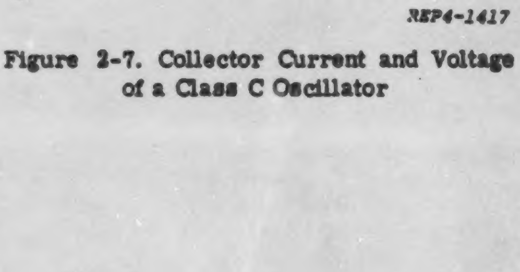
2-35. Figure 2-6 shows the Armstrong oscillator as you will probably see it. R3 has been added to improve temperature stability, C3 prevents degeneration, C4 is a coupling capacitor, and T2 provides a method of coupling the output signal. T2 is usually a loose-coupled *RF* transformer, which reduces undesired reflected impedance from the load back to the oscillator.

2-36. The Armstrong oscillator is an example of how a Class C amplifier can produce a sine-wave output that is not distorted. Although Class C operation is nonlinear and many harmonic frequencies are generated, only one frequency receives enough gain to cause the circuit to oscillate. This is the frequency of the resonant tank circuit. Thus, we can have high efficiency and an undistorted output signal.

2-37. The wave forms in Figure 2-7 illustrate the relationship between the collector voltage and collector current. Notice that collector current (I_C) flows for only a short time during each cycle. While the tank circuit is oscillating, L2 acts as the primary of a transformer and L1 acts as the secondary. The signal from the tank is, therefore, coupled through T1 to coupling capacitor C4, and the output collector voltage is a sine wave.

2-38. Before we troubleshoot the Armstrong oscillator, let's discuss some methods commonly used to determine if the circuit is operating. One method to check for circuit operation is to connect an oscilloscope to a point in the regenerative feedback loop. The presence of a signal indicates the circuit is oscillating. To prevent excessive loading on the circuit, the oscilloscope should be connected in shunt with the lowest impedance point in the circuit.

2-39. Another method of checking for oscillations is with a neon bulb. The oscillating circuit radiates electromagnetic energy. If a neon bulb is held physically close to the circuit, the neon will ionize and glow provided the oscillator can furnish the required power.



REP4-1417

Figure 2-7. Collector Current and Voltage of a Class C Oscillator

This check is not nearly as accurate as the oscilloscope because of many variables such as the size of neon bulb, strength of oscillator signal, and physical distance from the circuit. The neon bulb, however, is a quick way to check the circuit for operation. A third method used to check for oscillations is to measure the output with a high impedance AC voltmeter.

2-40. Troubleshooting an oscillator is relatively simple as long as you remember the requirements for an oscillator and the characteristics of an amplifier.

2-41. First, what malfunctions will prevent the amplifier from operating? Refer to Figure 2-6. If Q1 or R3 opens, the DC path for the transistor is broken. Q1 cannot amplify and the circuit cannot oscillate. If Q1 is shorted, the DC path is present but no amplification will be present, and there is no output from the circuit.

2-42. Second, what malfunctions can occur in the frequency determining device? With L2 or C1 shorted, no oscillations exist because the tank circuit is shorted to ground. If L2 opens, the resonant frequency of the tank goes to a higher value as determined by the capacitance between the open ends of the coil. If C1 opens, the resonant frequency of the tank goes to a higher value, because the resonant frequency is now determined by L2 and the shunt or distributed capacitance in the circuit. With L2 or C1 open, the oscillator may not operate because of the higher resonant frequency.

2-43. Third, in the regenerative feedback path, if C2 or L1 opens, the feedback is zero and the circuit will not oscillate.

2-44. Now, let's examine the remaining components. If R1 opens, the output amplitude will increase. If R1 is shorted, there is no output because there is no collector load impedance and no coupling to the tank circuit.

2-45. If R2 opens, we lose forward bias on Q1, and there may not be enough leakage current through Q1 to start the circuit oscillating. If R2 shorts, the excessive base current would probably damage the transistor.

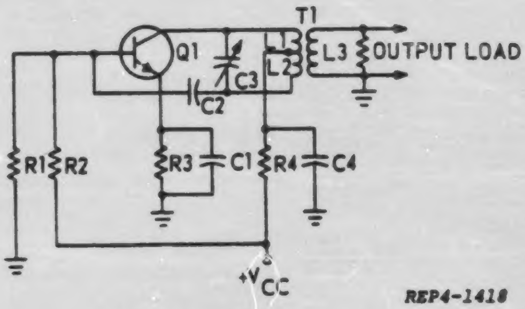


Figure 2-8. Series-fed Hartley Oscillator

2-46. If R3 or C3 shorts, the thermal stability is lost but the circuit will continue to operate as long as Q1 does not overheat. With C3 open, degeneration is present and the output amplitude will be smaller than normal or zero.

2-47. If C2 shorts, there may not be sufficient forward bias to start oscillations. This is because of the very low DC resistance of L2.

2-48. If C4 opens, the circuit continues to oscillate but there is no output signal. The same holds true if L3 or L4 opens.

2-49. If L3 or L4 were shorted, an excessive load would probably cause oscillations to dampen out. If C4 shorts, an excessive DC load is on the power supply (L1 and L3 in series) and the circuit would not oscillate.

2-50. There are many different oscillator circuits, so the troubles and symptoms listed here are general, and will vary with individual circuits. However, if you understand the principle of operation of an amplifier and the requirements for oscillation, troubleshooting the Armstrong oscillator should be quite easy.

2-51. Hartley Oscillator, Series Fed.

2-52. One of the most common oscillator circuits is the Hartley: Series fed and shunt fed. We will first discuss the series-fed Hartley oscillator. Refer to Figure 2-8 for the schematic diagram. The following list gives the purpose of the components:

R1 and R2	Voltage divider network for forward bias
R3	Swamping resistor for thermal stability
C1	Bypass capacitor for R3 to prevent degeneration
C2	Feedback coupling capacitor
C3, L1 and L2	Frequency determining device
L3	Coupling for the output circuit
R4 and C4	Low-pass filter network (decoupling network)

2-53. The identifying feature of a Hartley oscillator is the tapped coil. The oscillator is series fed because DC flows through the tank. Observe that DC flows from ground, through R3, Q1- L1, and R4 to +V_{CC}. When a part of the tank circuit is in series with the power supply so that DC flows through it, the circuit is said to be "series-fed." Regenerative feedback from the collector to the base of Q1 is through autotransformer action between L1 and L2.

2-54. To understand the circuit operation, assume the circuit is oscillating and the signal on the base (from the FDD) is going in a positive direction. The positive signal will cause the collector current to increase and the voltage across L1 will be negative at the top with respect to the tap. The voltage induced into L2 will be positive at the bottom with respect to the tap. This positive signal coupled back is in phase with the original signal, and it is regenerative. The negative alternation of the signal on the base causes collector current to decrease. This decrease in current will cause the voltage across L1 to go positive at the top with respect to the tap. The voltage induced into L2 will be negative at the bottom with respect to the tap. This negative signal is coupled through C2 to the Q1 base. Once again, the signal fed back is in phase with the original signal and, therefore, is regenerative.

2-55. The regenerative feedback path, then, is from the collector through L1 to L2, through C2 to the base. The amplitude of the feedback is controlled by the position of the tap. When the tap is moved down (making L1 larger and L2 smaller), the feedback amplitude decreases. When the tap is moved up, the feedback amplitude increases. The tap is positioned to send the correct amplitude of regenerative feedback to the base of the transistor as indicated by the shape of the output waveform. Observe that, regardless of the tap position, the frequency determining network does not change, so the output frequency does not change.

2-56. The low-pass filter network (R4-C4) is used for two purposes. First, the resistor drops V_{CC} to the desired value for the transistor. Second, the oscillator signal is isolated from the power supply by the large filter capacitor C4, connected between R4 and the tank circuit. The high frequencies will be shunted around the power supply, and the low frequencies (DC in this case) will pass on to the power supply.

2-57. Buffer Amplifier

2-58. Figure 2-8 shows the output circuit as a load placed on the frequency determining device. This type loading affects oscillator amplitude and frequency. A "buffer" amplifier decreases the loading effect on the oscillator by reducing interaction between the load and the oscillator.

2-59. Figure 2-9 is the schematic diagram of a buffer amplifier. This circuit is a common

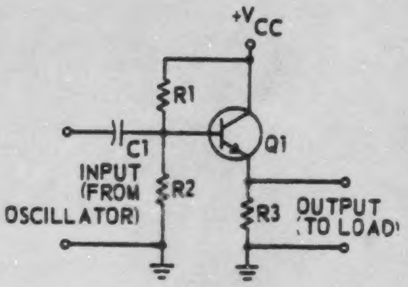


Figure 2-9. Buffer Amplifier

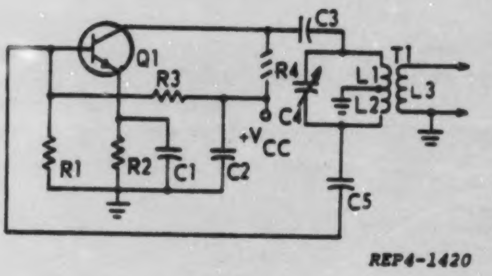


Figure 2-10. Shunt-fed Hartley Oscillator

collector amplifier. A common collector has a high input impedance and a low output impedance. Since the output of the oscillator is connected to the high input impedance of the common collector, the buffer has little effect on the operation of the oscillator. The output of the common collector is then connected to an external load, with the result that changes in the output load cannot reflect back to the oscillator circuit. Thus, the buffer amplifier reduces interaction between the load and oscillator. This is "one-way" coupling since the oscillator signal is coupled forward, but load changes are not coupled back to the oscillator.

2-60. Hartley Oscillator, Shunt Fed.

2-61. The second Hartley oscillator is the shunt-fed type. Figure 2-10 shows the schematic diagram. Again, we find a tapped coil -- the identifying feature of a Hartley oscillator. The frequency determining device (C4, L1, and L2) is now in shunt with the DC path through the amplifier (ground, R2, Q1, and R4 to V_{CC}).

2-62. The following list shows the purpose of the components:

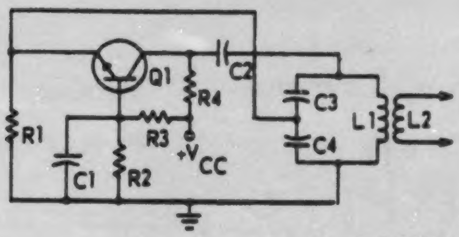
R1 and R3	Voltage divider network for forward bias
R2	Swamping resistor for thermal stability.
C1	Bypass capacitor to prevent degeneration
C2	Decoupling capacitor for the power source
R4	Collector load resistor
C3	Coupling capacitor
C5	Feedback coupling capacitor
C4, L1, and L2	Frequency determining device
L3	Coupling for the output circuit

2-63. Coupling capacitors C3 and C5 block DC from the tank circuit; thus, the oscillator is "shunt fed." Regenerative feedback from the collector to the base of Q1 is through C3, autotransformer action between L1 and L2 and through capacitor C5.

2-64. To understand the circuit operation, assume that the circuit is operating and the signal on the base is going positive. The positive signal will cause collector current to increase and collector voltage to decrease (go in a negative direction). This negative-going signal couples through C3, and the voltage across L1 will be negative at the top with respect to the tap. The voltage induced into L2, then, will be positive at the bottom with respect to the tap. This positive-going signal is then coupled through C5 to the base. Since the signal coupled back is in phase with the original signal, it is regenerative.

2-65. The negative alternation of the signal on the base causes collector current to decrease and the collector voltage to increase (go in a positive direction). This positive-going signal couples through C3, and the voltage across L1 will be positive at the top with respect to the tap. The voltage induced into L2, then, will be negative at the bottom with respect to the tap. This negative-going signal is then coupled through C5 to the base. Once again, the signal fed back is in phase with the original signal and, therefore, is regenerative.

2-66. The regenerative feedback path, then, is from the collector through C3 to L1, to L2 through C5 to the base. Once again,



REP4-1421

Figure 2-11. Colpitts Oscillator

the position of the tap determines the amount of feedback in the circuit. Use Figure 2-10 to troubleshoot the shunt-fed Hartley oscillator. Assume Class A operation.

Symptom: No output and V_C is zero volts; the possible troubles include R4 open, C2 shorted, or C3 shorted.

Symptom: No output and V_C is normal; the possible trouble could be C5 open, C3 open, the tap on L1-L2 not grounded, or C1 open.

Symptom: No output and V_C approximately equal to V_{CC}; the trouble now could be R2 open, R3 open, R1 shorted, C5 shorted, or R4 shorted.

2-67. Colpitts Oscillator

2-68. Another typical oscillator is the Colpitts. Figure 2-11 shows the schematic diagram. The identifying feature of this oscillator is a split capacitor. The following list gives the purpose of the components:

R1	Emitter resistor to develop the feedback signal.
R2 and R3	Voltage divider network for forward bias
C1	Base bypass capacitor that keeps the base at AC ground
R4	Collector load resistor
C2	Coupling capacitor between the collector and the tank
C3, C4, and L1	Frequency determining device
L2	Output coupling device

2-69. The two capacitors (C3 and C4) in the frequency determining device provide the Colpitts oscillator with capacitive feedback. As the Hartley oscillators use a tapped coil for inductive feedback, Colpitts oscillators use split capacitors for capacitive feedback. Before discussing the operation of the two capacitors, let's trace the regenerative feedback path.

2-70. Starting at the collector of Q1, the feedback goes through C2, to the tank circuit, and from the connection between the two capacitors to the emitter of Q1. Q1 is connected in a common base configuration and does not phase shift the signal, neither does the tank circuit. So, the feedback is reremerative.

2-71. To illustrate the purpose of the two capacitors, C3 and C4, refer to Figure 2-12, a rearrangement of components from Figure 2-11. This shows only the emitter-to-base circuit with respect to the tank circuit. Notice the interelement capacitance between the emitter and base C_{eb}.

2-72. When a tank circuit is connected across a junction of a transistor, the transistor interelement capacitance becomes part of the

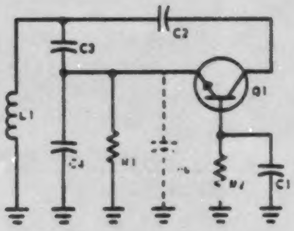
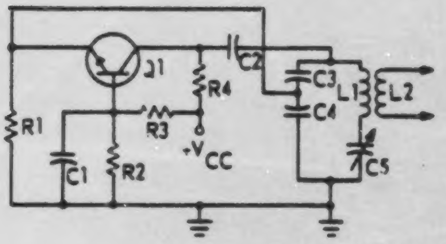


Figure 2-12. Colpitts Oscillator; Emitter Circuit Redrawn



REP4-1423

Figure 2-13. Clapp Oscillator

tank capacitance. If this interelement capacitance changes, the frequency of the tank circuit will change. Among other things, heat and the amount of bias affect the capacitance between the transistor elements; therefore, C_{eb} is subject to change. In the Colpitts oscillator, one of the two capacitors in the tank circuit, C4 , is connected across the emitter-base junction. This connection places C_{eb} in parallel with C4. To decrease the effects of a change in C_{eb}, we select a size for C4 that will make it much larger than C_{eb}. For example, if C_{eb} is 10 picofarads, then select 1000 picofarads for C4. The total parallel capacitance of C_{eb} and C4 would be 1010 picofarads. The size of C3 is selected to make the circuit resonate with L1 at the desired frequency. Let's assume that C3 is 100 picofarads. The total tank capacitance is about 90.9 picofarads.

2-73. To illustrate our example, let's assume that the interelement capacitance increases 100 percent to 20 picofarads. How much does the total tank capacitance change? We find that the total tank capacitance is now about 91.1 picofarads. This represents a change in total tank capacitance of about 0.2 percent. So, with a 100 percent change in interelement capacitance the resonant frequency changes less than 0.2 percent. By a more careful selection of component sizes, an even smaller degree of change can be achieved. Using two capacitors reduces the undesirable effect of transistor interelement capacitance changes on the frequency determining device. This allows the Colpitts oscillator to have good frequency stability characteristics. The two capacitors also act as a voltage divider to insure the correct amplitude of feedback.

2-74. The Colpitts oscillator may be tuned by varying the inductance or capacitance. However, when capacitance tuning is used, both capacitors must be tuned at the same time. Since C3 and C4 (Figure 2-12) form a voltage divider network for the regenerative feedback if one capacitor is varied, the ratio of C3 and C4 changes and the amount of feedback changes. To maintain the ratio and thus reduce the possibility of distortion or loss of oscillations, capacitors connected on the same shaft (ganged capacitors) are used with capacitive tuning.

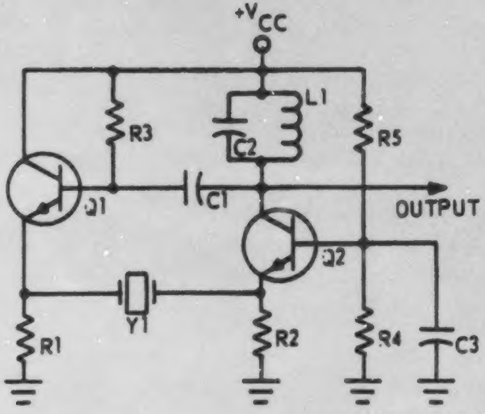
2-75. Clapp Oscillator

2-76. The Clapp oscillator (Figure 2-13) is a modified Colpitts oscillator. Tuning capacitor C5 is added in series with the tank inductance so that the frequency determining device now consists of C3, C4, C5, and L1. Like the Colpitts, the Clapp oscillator reduces the effects of transistor interelement capacitance. Using the single tuning capacitor makes this oscillator much easier to tune than the Colpitts.

2-77. Another advantage of the Clapp oscillator is the reduction of "hand capacitance." When you place your hand near the tuning device, the capacitance of your hand and body may cause the frequency of an oscillator to change. One plate of tuning capacitor C5 is at ground potential; this reduces the effect of hand capacitance.

2-78. To troubleshoot the Clapp oscillator, assume Class a operation.

Symptom:	No output and V_C is low
Cause:	C4 shorted, R1 short, or possibly R2 open
Symptom:	The output frequency is lower than normal
Cause:	C5 shorted



REP4-1424

Figure 2-14. Butler Oscillator

Symptom:	No output and V_C is normal
Cause:	C2 open, C3 open, C4 open, L1 open or shorted, C5 open, L2 open or shorted

2-79. Butler Oscillator

2-80. The Butler oscillator, shown in Figure 2-14, has two primary identifying features. Two transistors are used, and a crystal is connected between the emitters. The purpose of the components are listed below:

R1	Emitter resistor of Q1, develops the output of Q1
R2	Emitter resistor of Q2, develops the input signal to Q2
Y1	Frequency determining device
R4 and R5	Forward bias voltage divider for Q2
C3	Base bypass capacitor for Q2
L1 and C2	Resonant tank load impedance for collector of Q2
C1	Coupling capacitor
R3	Forward bias resistor for Q1

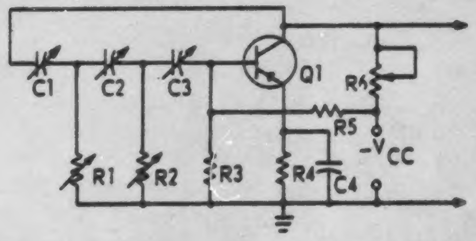
2-81. Q1 is a common collector configuration and Q2 is a common base configuration. The regenerative feedback path is: From the collector of Q2, through C1 to the base of Q1, to the emitter of Q1, through the crystal Y1, and back to the emitter of Q2. The regenerative feedback must pass through the crystal. At its resonant frequency, the crystal has a very low impedance and will pass the feedback signal to the emitter of Q2. All other frequencies will be blocked because of the high impedance of the crystal.

2-82. The output signal from the circuit can be obtained directly from the collector of Q2. The tank circuit, L1 and C2, will flywheel and produce a signal on the collector. At the same time the cyrstal is vibrating to produce a signal on the emitter of Q2. With both transistors operated Class C, Q2 will be cut off for a majority of the time. This condition provides buffer action between the collector circuit of Q2 and the crystal. When the output is taken from the collector, the external load will have very little effect on the crystal operation. This eliminates the need for another circuit to provide buffer action. Remember, the frequency determining device is the crystal and NOT L1 and C2. The L1 and C2 resonant frequency should be near that of the crystal. When both transistors are operated Class A, L1 and C2 can be replaced by a resistor.

2-83. Phase Shift Oscillator

2-84. Resistive capacitive networks provide regenerative feedback and determine the frequency of operation in RC oscillators.

2-85. A phase shift RC oscillator circuit is shown in Figure 2-15. The following list gives the purpose of the components:



REP4-1425

Figure 2-15. Phase Shift Oscillator

R1, R2, R3, C1, C2 + C3	Phase shifting network and frequency determining device
R5 and R3	Voltage divider network for forward bias
R4 and C4	Emitter swamping resistor and bypass capacitor
R6	Collector load resistor (Feedback amplitude control)

2-86. In Figure 2-15, notice the arrangement of the three RC networks. C1 and R1 form the first RC network, C2 and R2 form the second, and C3 and R3 form the third. Resistor R5 provides forward bias voltage and is much larger than R3.

2-87. The input signal to the RC networks is from the collector of Q1, and the output signal from the RC networks is applied to the base of Q1. Q1, a common emitter configuration, has a 180-degree phase shift from base to collector. To obtain regenerative feedback for sustained oscillations, the collector signal of Q1 must be shifted 180 degrees before it is returned to the base of Q1. This is accomplished by the three RC networks. To get 180 degrees from a three-section network, each section provides approximately 60 degrees phase shift. The capacitors and resistors in the RC networks may be adjusted to provide the required phase shift for the desired frequency. The collector signal is thus shifted a total of 180 degrees and returned to the base of Q1 as regenerative feedback.

2-88. But what about the frequencies above and below the desired operating frequency? Remember, if capacitance and resistance are held constant, the amount of phase shift per section depends upon frequency. All frequencies above the desired operating frequency will be phase-shifted less than 180 degrees and will not be regeneratively fed back. Also, all frequencies below the desired operating frequency will be phase shifted more than 180 degrees and feedback will not be regenerative. Only one frequency will have the correct 180-degree phase shift to provide regenerative feedback for the circuit.

2-89. Transistor amplifier Q1 must operate Class A because the RC frequency determining device has no flywheel action. Recall how LC oscillators maintain a sine-wave output even though they operate Class C, because of the tank-circuit flywheel action. For a sine-wave output from the phase shift oscillator, transistor Q1 must conduct 360° of the cycle, and operate in the linear portion of its characteristic curve. If the regenerative feedback is too small, the circuit will not oscillate; if the regenerative feedback is too large, distortion will be present in the output. The collector load resistor, R6 in Figure 2-15, is variable to allow adjustment of the feedback. By decreasing R6, the voltage gain of the circuit decreases and the amplitude of the feedback is reduced. In some circuits, the emitter resistor is unbypassed and variable to allow some degeneration to be present to insure an undistorted output signal.

2-90. To determine the frequency of operation use the formula:

$$F_o = \frac{1}{2\pi RC \sqrt{2N}}$$

where N is the number of RC sections. Figure 2-15 uses three sections so the formula becomes:

$$F_o = \frac{1}{2\pi RC \sqrt{2(3)}}.$$

2-91. Now, let's consider troubleshooting:

Symptom:

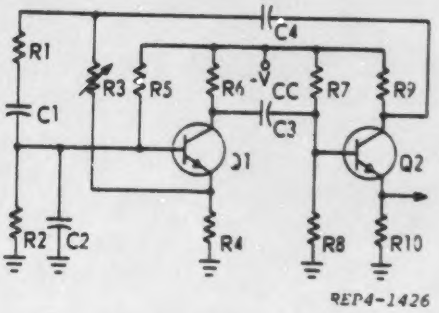


Figure 2-16. Wien Bridge Oscillator

Symptom: No output and V_C is normal

Probable cause: C1, C2, C3, R1, or R2 could be open or C2, R1, or R2 could be shorted

Symptom: No output and V_C is higher than normal

Most likely cause: C3 shorted

2-92. Wien Bridge Oscillator

2-93. The Wien bridge oscillator is another RC oscillator. It uses two transistor amplifiers and a bridge circuit for feedback. It also uses the phase shift characteristics of RC networks. The following list gives the purpose of components. Refer to figure 2-16.

R1-C1, R2, & C2	Frequency determining device
R3-R4	Degenerative feedback network
R2-R5 & R7-R8	Amplifier forward bias networks
R6 & R9	Collector load resistors
C3 & C4	Coupling capacitors
R10	Emitter resistor which develops the output

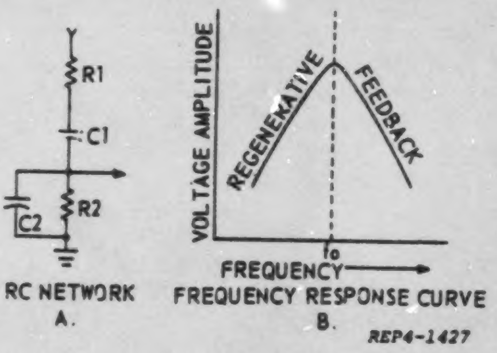
2-94. The frequency determining device (R1, C1, R2, and C2) is a series-parallel RC network. Any voltage that is developed across parallel R2 and C2 is applied to the base of Q1, and any voltage developed across R4 in the R3-R4 voltage divider network is applied to the emitter of Q1. So, during normal operation, there are two signals applied to Q1 at the same time. Degenerative feedback network R3-R4 is not frequency selective. Any signal coupled from the collector of Q2, through C4, will appear on the emitter of Q1 with a reduced amplitude. The frequency determining network IS frequency selective. The amplitude of the signal on he base of Q1 depends on the frequency of the signal. Due to this arrangement, one frequency will cause a larger voltage on the base of Q1 (across R2 and C2) than any other. This is the oscillator operating frequency.

2-95. To illustrate the operation of the Wien bridge oscillator frequency determining device, refer to Figure 2-17. First, let's assume that R1 is equal to R2, and C1 is equal to C2. Maximum amplitude will be developed across parallel branch R2 and C2 at the center frequency.

2-96. At frequencies above F_o, the impedance of the R2-C2 network decreases more than the impedance of the R1-C1 network. This will reduce the amplitude of the signal developed across R2-C2.

2-97. At frequencies below F_o, the impedance of the R1-C1 network increases more than the impedance of the R2-C2 network. This will decrease the amplitude of the signal across R2-C2. (Notice the frequency response curve in Figure 2-17B).

2-98. The signal across the R2-C2 section not only varies in amplitude with a frequency change but also varies in phase. At the frequency of operation, F_o, the current in the series-parallel frequency determining network, leads the applied voltage by 45 degrees. However, the parallel section has a lagging impedance of 45 degrees. For the parallel portion, then, a plus 45-degree current and a minus 45-degree impedance give a voltage of zero degrees $(I\angle +45^\circ \times Z\angle -45^\circ = E\angle 0^\circ)$. This makes the voltage applied to the base of Q1 in phase and regenerative. At frequencies above and below F_o, the feedback signal will not be of the proper phase to sustain oscillations. So, for given values



RC NETWORK A.

FREQUENCY RESPONSE CURVE B.

Figure 2-17. Frequency Determining Device; Wien Bridge Oscillator

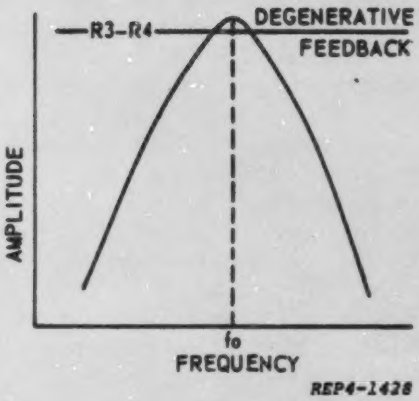


Figure 2-18. Degenerative Feedback Diagram

in the frequency determining network, only one frequency, F_O, will have a feedback signal that is of proper phase. Both Q1 and Q2 invert the signal making a 360-degree phase shift. The Q2 collector voltage is, therefore, in phase with the Q1 base signal.

2-99. This characteristic of the RC frequency determining device allows maximum regenerative feedback for only one frequency. A small amount of degenerative feedback increases the frequency stability of the circuit. Network R3-R4 provides this signal to the emitter of Q1. Now, refer to Figure 2-18.

2-100. Since resistors R3 and R4 are not frequency sensitive, they pass all frequencies. Notice that there is only a small area where the regenerative feedback is higher in amplitude than the degenerative feedback. Since sustained oscillations require regenerative feedback, the circuit will only operate at the frequency where this occurs.

2-101. Tuning the circuit requires the adjustment of some part of the frequency determining device. The usual tuning method is to use ganged capacitors (C1 and C2) or ganged resistors (R1 and R2).

2-102. Sometimes R3 (Figure 2-16) is made variable to adjust degenerative feedback. Increasing R3 reduces degenerative feedback. This would cause the output signal amplitude to increase and possibly become distorted. Decreasing R3 increases degenerative feedback and reduces the output signal amplitude. Decreasing R3 further may stop the oscillator. Therefore, R3 is adjusted for maximum output amplitude with minimum distortion.

2-103. To determine the frequency of operation, F_O, use the following formula:

$$F_O = \frac{1}{2\pi \sqrt{(R1)\ (R2)\ (C2)\ (C1)}}$$

When R1 equals R2 and C1 equals C2, the formula reduces to

$$F_O = \frac{1}{2\pi RC} \quad \text{or} \quad \frac{.159}{RC}.$$

In troubleshooting the Wien Bridge oscillator, we must consider that we have two amplifiers, two feedback loops, and a frequency determining device. With no output, a check of collector voltage of each transistor would identify if the trouble was in the DC circuit of the transistors. If the following symptoms were present, we would look for the following troubles. Use Figure 2-16.

SYMPTOM	POSSIBLE TROUBLE
V_C Q1 High No Output	R6 short, R4 open, R5 open, R2 short, C2 short
V_C Q1 Low	R6 open, R4 short, R5 short, R2 open
V_C Q2 High No Output	R9 short, R10 open, R8 short, R7 open
V_C Q2 Low	R7 short, R8 open R10 short, R9 open, C3 short
V_C Q1 & Q2 No Output	C3 open, C4 open, R1 open or short C1 open or short, C2 open, R3 short
Output Amplitude High and Frequency Unstable	R3 open

2-104. Frequency Multipliers

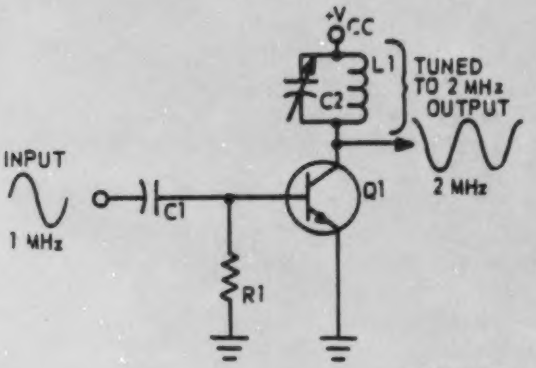


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Figure 2-19. Frequency Multiplier

2-105. To obtain higher frequencies than the resonant frequency of an oscillator, the oscillator output can be fed to a frequency multiplier. As the name implies, a frequency multiplier circuit is one whose output frequency is some multiple of the input frequency. For example, a frequency doubler will double the input frequency, a tripler will triple the frequency, and a quadrupler will multiply the input frequency by four.

2-106. To multiply a frequency, a circuit must generate harmonic frequencies in the output. This requires Class B or Class C amplifier operation. Figure 2-19 is the schematic diagram of a frequency multiplier, a doubler in this example. Assume Q1 operates Class C. Q1 is cut off with no input signal because it has no forward bias. During the positive alternation of the input signal, Q1 is forward biased by the signal and coupling capacitor C1 charges rapidly. Once the capacitor is charged and the input signal starts in the negative direction, the transistor is cut off. The only discharge path for C1 is through R1. This is a long time constant so C1 cannot discharge very fast. The average voltage on C1 becomes the reverse bias for the base-emitter junction and allows Class C operation for the transistor. Of necessity, the input signal must be larger than that normally applied to an amplifier circuit.

2-107. With Class C operation, the transistor will generate many harmonics of the input signal. The output signal is the harmonic to which the collector tank circuit is tuned. In Figure 2-19, the tank circuit is tuned to the second harmonic of the input signal. With 1 megahertz input, the output signal will be a sine-wave signal of 2 megahertz.

2-108. If the collector tank were tuned to 3 megahertz, the third harmonic of the input signal, the output would be 3 megahertz. The same is true with the fourth harmonic. The fourth harmonic, or frequency quadrupler, is normally as high in multiplication as practical, because as you tune to higher harmonics, the output signal becomes weaker. Two doublers are often more desirable than one quadrupler. Although each will produce the same frequency multiplication, two doublers provide more power in the output signal.

2-109. If the input frequency and the component values of the tank circuit are known, you can determine whether the stage is a doubler or tripler. For example, if the input signal is 10 MHz, would a .016 millihenry inductor and a 4-picofarad capacitor form a frequency doubler or tripler? Using the formula

$$f_r = \frac{.159}{\sqrt{LC}}$$

we find the tank circuit's resonant frequency.

$$f_r = \frac{.159}{\sqrt{.016 \times 10^{-3} \times 4 \times 10^{-12}}} =$$

$$\frac{.159}{\sqrt{.064 \times 10^{-15}}} = \frac{.159}{\sqrt{64 \times 10^{-18}}} =$$

$$\frac{.159}{8 \times 10^{-9}} = 19.9 \text{ or } 20 \text{ MHz.}$$

So these tank component values make a frequency doubler. In a problem of this type, rounding off .159 to .16 will simplify the calculations.

2-110. Another feature of frequency multipliers is that they provide the characteristics of a buffer amplifier. Since the transistor is operated Class C, the load on the multiplier does not reflect impedance back to the base circuit. And, because of Class C

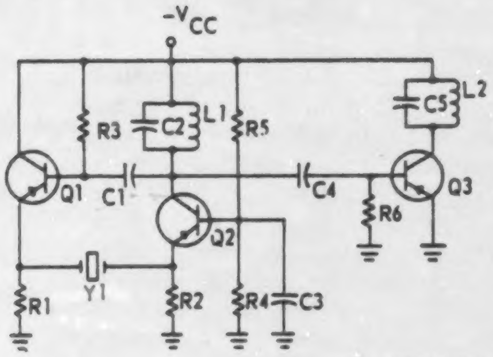

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Figure 2-20. Butler Oscillator and Frequency Multiplier

operation, the input impedance to the base is relatively high (the base-emitter junction is reverse biased most of the time).

2-111. Figure 2-20 shows the schematic diagram of a Butler oscillator connected to a frequency multiplier. Q3 and its circuitry are the frequency multiplier, which also serves as buffer amplifier for the oscillator.

2-112. Another characteristic of frequency multipliers concerns neutralization and unilateralization. Since the input frequency and output frequency of a multiplier are different, there is usually no need for unilateralization or neutralization of the circuit. Any feedback through the transistor would not be in phase, so the frequency multiplier could not oscillate.

Chapter 3

PULSED OSCILLATORS

3-1. A conventional sinusoidal oscillator is one that will produce output pulses at a predetermined frequency for an indefinite period of time. That is, it operates continuously. Many electronic circuits require that an oscillator be turned on for a specific time duration, and then remain in an off condition until required at a later time. These circuits are called pulsed oscillators. They are nothing more than sine-wave oscillators that are turned on and off at specific times.

3-2. There are two primary classifications of pulsed oscillators. One is classified as having regenerative feedback and the other without regenerative feedback. Both will be discussed in the following section.

3-3. A pulsed oscillator is a form of ringing circuit so we will discuss ringing circuits in general before going into the oscillator. A ringing circuit is a resonant circuit which is excited into oscillation and allowed to oscillate or "ring" without feedback until oscillations die out.

3-4. Figure 3-1A shows a parallel resonant circuit connected to a DC source through a switch (S1) and a current limiting Resistor (R1). With S1 closed, a DC current flows from ground through R_{DC}, L1, S1, and R1 to the positive voltage source. The DC resistance of L1 (R_{DC}) is low, so a small voltage will be dropped across L1. Due to the current flow, a magnetic field will be built up around L1. The field will not collapse as long as a steady direct current exists and, therefore, no flywheel action can take place.

3-5. Assume that at time T_0, in Figure 3-1B, we open S1. The field around L1 collapses, inducing a voltage to keep current flowing in the same direction. Thus, the voltage polarity across L1 reverses, current flows to charge C1, and flywheel action begins. The circuit will oscillate at a frequency determined by L1 and C1.

3-6. The waveform in Figure 3-1B shows that the amplitude of oscillations decreases during the time S1 is open (T_0 to T_1). This is due to the power being dissipated as the current circulates, with no provision for replacing the lost power. R_{AC} is an equivalent resistance representing all of the power-dissipating elements in the tank. The higher the Q, the less the loss, and the slower the rate of decline in amplitude. If a variable resistance were placed in shunt with the tank, the rate of decline could be controlled. This is true because

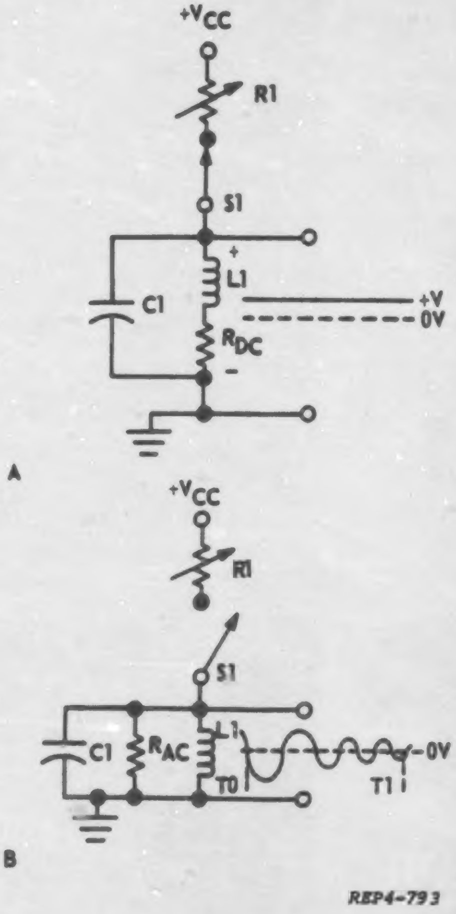

Figure 3-1. Basic Ringing Circuit

$Q = \frac{R_{AC}}{X_L}$. The greater the R, the greater the Q, and the slower the rate of decline.

3-7. The polarity of the first alternation of a pulsed oscillator will depend on the direction of the initial current through the coil with respect to ground. The amplitude of the first alternation is a function of the current at the time S1 is opened and the reactance of L1 at the resonant frequency. With R1 smaller, a larger current would flow through L1; more current through L1 would induce a larger voltage when the switch is opened. By adjusting R1, therefore, the amplitude of the first alternation is controllable.

3-8. Figure 3-2 shows a pulsed oscillator with the resonant tank in the emitter circuit. It is actually the same circuit as Figure 3-1, except that the adjustable resistor is removed and S1 has been replaced with Q1. A positive input makes Q1 conduct heavily, current flows through L1; and no oscillations take place. A negative gate cuts Q1 off, and the tank will oscillate until the gate ends (or until the ringing stops, whichever comes first).

3-9. In Figure 3-2, R1 provides the forward bias voltage for Q1. L1 and C2 form the resonant tank circuit. Q1 serves as the current limiting resistance, and the bias on Q1 controls the amplitude of the first alternation of the output. The more forward bias on Q1, the larger the amplitude of the frst alternation.

3-10. The waveforms in Figure 3-2 show the relationship of the input gate and the output signal from the pulsed oscillator. Assume that the Q of the LC tank circuit is high enough to prevent damping. An output from the circuit is obtained when the input gate goes negative. To to T1, and T2 to T3. The remainder of the time, T1 and T2, the transistor conducts heavily and there is no output from the circuit. The width of the input gate controls the time for the output signal. By making the gate length longer, an output is present for a longer time.

3-11. It is relatively simple to calculate the number of cycles present in the output when the gate length and resonant frequency are known.

3-12. For example, if the tank circuit is resonant at 1 megahertz, and the gate length on the negative alternation is 500 microseconds, then there will be 500 cycles of one megahertz present in the output. Let's check this by converting frequency to time, using

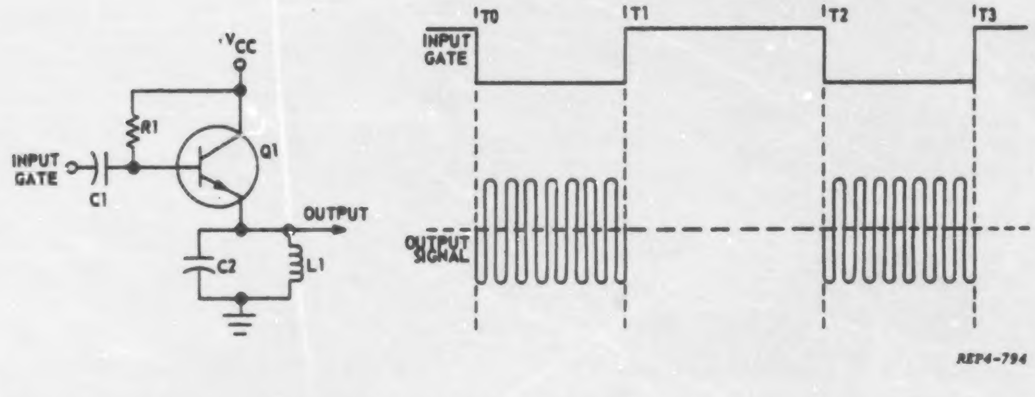

Figure 3-2. Emitter Loaded Pulsed Oscillator

$t = \frac{1}{f}$. One cycle of a megahertz requires one microsecond of time. Then, dividing the time for one cycle (one microsecond) into the gate length (500 microseconds), we get the number of cycles (500).

3-13. Another version of the pulsed oscillator is shown in Figure 3-3. Compare this with Figure 3-2; this time the tank has been placed in the collector circuit. R1 provides the forward bias for the transistor, C2 and L1 the frequency of the output sine wave. C1 is a coupling capacitor to allow the input gate to be applied to the circuit.

3-14. The primary difference between the tank in the emitter or in the collector is the polarity of the first alternation of the output. Recall the basic principle of induction; any change in magnetic field induces a voltage which opposes the change. In Figure 3-3, current flows from the emitter to the collector of Q1 through L1, to $+V_{CC}$. When Q1 is cut off by the negative alternation of the input gate, collector current will stop. Due to the collapsing field around L1, the voltage produced will be of the polarity to cause current to continue in the same direction. This will cause the collector to go positive, making the first output alternation positive.

3-15. Refer to Figure 3-2 and you should be able to see why the first alternation is negative. Suppose Q1 is a PNP transistor with V_{CC} negative. Current flow from $-V_{CC}$ to ground causes the first alternation to go in a positive direction. Now, refer to Figure 3-3 and replace the NPN with a PNP, and change the polarity of V_{CC}. The polarity of the first output alternation is negative.

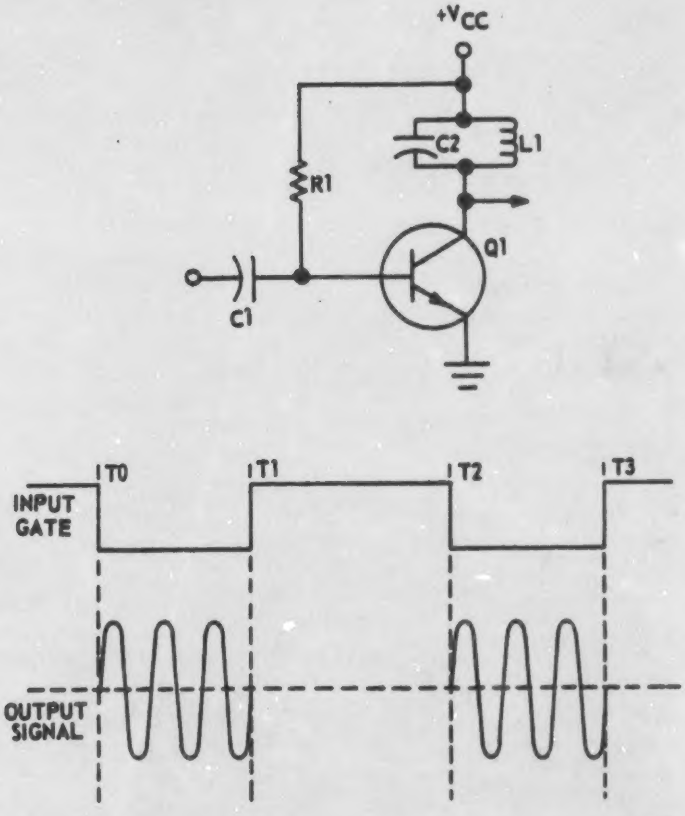

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Figure 3-3. Collector Loaded Pulsed Oscillator

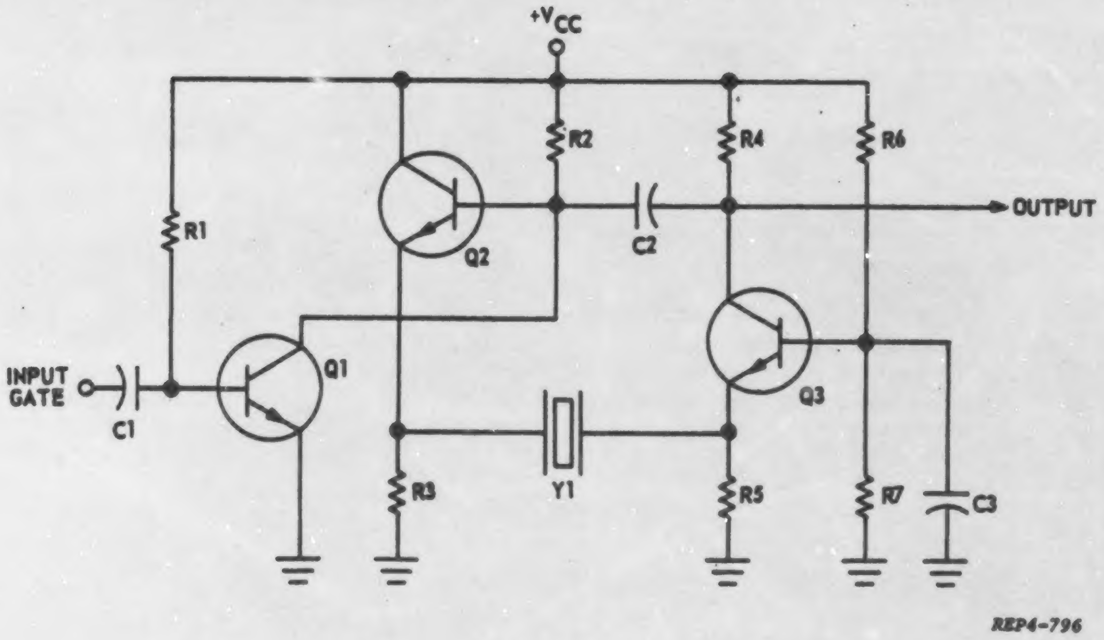

Figure 3-4. Pulsed Oscillator

3-16. Observe that the waveshapes in both figures 3-2 and 3-3 have no damping. Actually, the output of a pulsed oscillator WITHOUT regeneration is a damped wave, the duration of which is controlled by the input gate length.

3-17. The second classification of pulsed oscillators is one WITH regenerative feedback (has no damping). This type consists of continuous sine-wave oscillator circuit producing a sine-wave output signal.

3-18. Figure 3-4 shows a Butler oscillator (Class A operation) that has been modified to allow pulsing. Q2 and Q3 are the Butler oscillator transistors. Y1 connects the two emitters and determines the output frequency. Refer to chapter 2 for a review of this type oscillator operation. Transistor Q1, resistor R1, and capacitor C1 have been added to provide a means of applying gates to the oscillator circuit. R2 (which provides bias for Q2 in the basic oscillator circuit) now has a second purpose; R2 is the collector load resistor for Q1. The Q1 collector current flows through R2, which drops most of the V_{CC} voltage. The voltage on the collector of Q1, which is also the base of Q2, is so small that Q2 is at cutoff. With Q2 cut off, the path for regenerative feedback for the oscillator is broken and the circuit will not oscillate. Q1 conducting keeps the oscillator in an "off" condition.

3-19. A negative gate coupled to the base of Q1 cuts it off. With Q1 cut off, the voltage on the base of Q2 returns to a forward bias value determined by R2. The Butler oscillator now operates, developing an output at the collector of Q3.

3-20. One advantage of the pulsed oscillator with regenerative feedback is that the output sine wave is not damped; the peak output will have the same amplitude for every cycle. This feature becomes important when many cycles of the output signal are required.

65

Chapter 4

BLOCKING OSCILLATORS

4-1. The blocking oscillator is a special type of wave generator used to produce a narrow pulse, sometimes called a trigger. Blocking oscillators have many uses, most of which are concerned with the timing of some other circuit. They can be used as frequency dividers or counter circuits and for switching other circuits on and off at specific times. This chapter discusses a basic blocking oscillator circuit and its output wayeforms.

4-2. Before going into the blocking oscillator circuit, several general considerations which apply to all blocking oscillators need to be discussed.

4-3. First, the timing pulses of electronic circuits have strict requirements. The times involved vary from a few hundredths of a microsecond to several thousand micro seconds.

4-4. Figure 4-1 shows two timing pulses. The basic requirements are:

1. Fast rise time.
2. Flat top.
3. Fast fall time.
4. Specific and accurately controllable frequency.

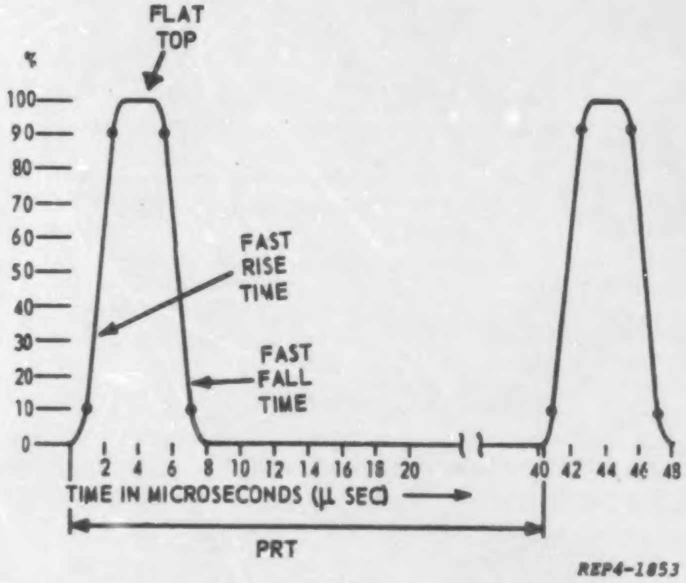

Figure 4-1. Timing Pulses

4-5. The leading edge of the pulse should be as steep as possible; that is, the rise time should be short. The top of the pulse should be as flat as possible, especially when the duration is long.

4-6. The trailing edge of the pulse should also be as steep as possible; that is, the fall time should be short. The PRT should be stable and accurately controllable because it determines the pulse recurrence frequency (PRF).

4-7. PW (pulse width) may be thought of as being the duration in time - usually expressed in microseconds - of a pulse, the measurement being made at 70% of the peak amplitude. PRT (pulse recurrence time) is the time (usually expressed in microseconds) between the beginning of two successive pulses. PRF (pulse recurrence frequency) is the number of pulses per second, and is the reciprocal of the PRT. In a free-running blocking oscillator, the PW, PRT, and PRF are all controlled by the size of certain resistors and capacitors, and the operating characteristics of the transformer. The transformer primary determines the duration and shape of the output. Because of its importance in the circuit, let's briefly discuss transformer action and review series RL circuits.

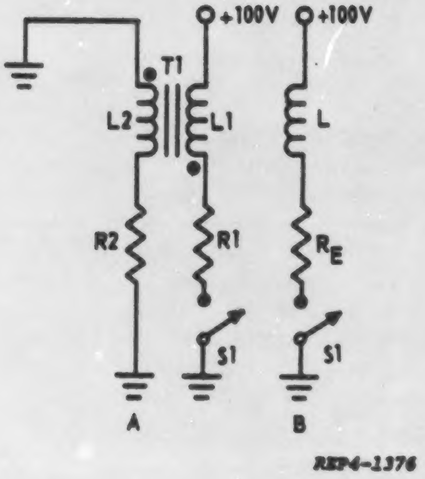

Figure 4-2. RL Circuits

4-8. Figure 4-2A shows a transformer with resistance in both the primary and secondary circuits. If S1 is closed, current will flow through R1 and L1. As the current rises, it induces a voltage into L2 and a current flows through R2. The voltage across L2 depends on the turns ratio between L1 and L2.

4-9. The secondary load impedance, R2, will affect the primary impedance through reflection from secondary to primary. If we increase the load on the secondary (decrease R2), we also increase the load on the primary. Similarly, if we decrease R1, primary and secondary currents increase.

4-10. Since T1 has an effective inductance and any change in R1 or R2 will change the current, we can show T1 as an inductor and R1-R2 as a combined or equivalent series resistance. The equivalent circuit is shown in Figure 4-2B. It acts as a simple series RL circuit, and we can discuss it in those terms.

4-11. In the simple series RL circuit, when S1 is closed, L acts as an open at the first instant and the source voltage appears across it. As current begins to flow, E_L decreases and E_R and I increase, all at exponential rates. Figure 4-3A shows these curves. In a time equal to 5 TIME CONSTANTS (5 x $\frac{L}{R_E}$) the resistor voltage and current will be maximum, and E_L zero.

4-12. If we close S1 in Figure 4-2B the current will follow curve 1 of Figure 4-3A. The time required for the current to reach maximum depends on the size of L and R_E. If R_E is small, then we have a long time constant RL circuit. If we use only a small portion of Curve 1 (A to B) then the current rise would have maximum change in a given time period. Further, the smaller the time increment, the more nearly linear is the current rise. A constant current rise through the coil is a key factor in a blocking oscillator.

4-13. A basic principle of inductance is that, if the rise of current through a coil is linear, that is, the rate of current rise is constant

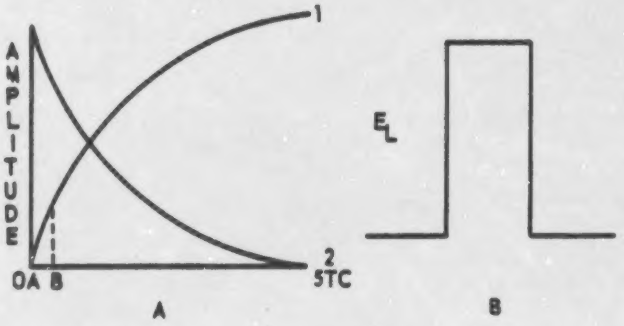

Figure 4-3. Voltage Across a Coil

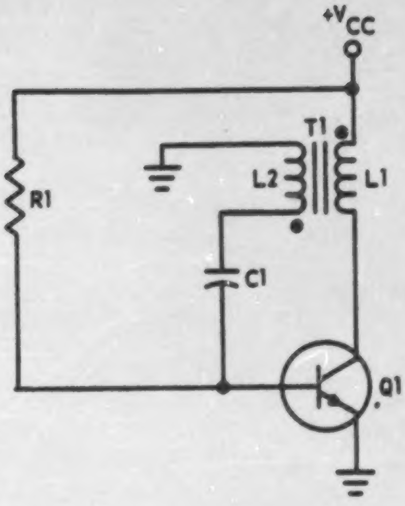

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Figure 4-4. Blocking Oscillator

with respect to time, then the induced voltage will be constant. This is true in both the primary and secondary of a transformer. Figure 4-3B shows the voltage across the coil when the current through it rises at a constant rate. Notice that this is similar in shape to the timing pulse in Figure 4-1.

4-14. Now, we are ready to discuss a blocking oscillator circuit. By definition, a blocking oscillator is a special type of oscillator which uses inductive regenerative feedback, with output duration and frequency determined by the characteristics of a transformer and its relationship to the circuit. Figure 4-4 shows the schematic diagram of a blocking oscillator. This is a simplified form used to discuss circuit operation.

4-15. When power is applied to the circuit in Figure 4-4, R1 provides forward bias and transistor Q1 conducts. Current flow through Q1 and the primary of T1 induces a voltage in L2. The phasing dots on the transformer indicate a 180-degree phase shift. So, as the bottom side of L1 is going negative, the bottom side of L2 is going positive. The positive voltage of L2 is coupled to the base of the transistor through C1, and Q1 conducts harder. This provides more collector current and more current through L1. This action is regenerative feedback. Very rapidly a voltage is applied to the base of the transistor that is sufficient to saturate the base. Once the base becomes saturated, it loses control over collector current. The circuit now can be compared to a small resistor (Q1) in series with a relatively large inductor (L1) or a series R1 circuit.

4-16. The operation of the circuit to this point has generated a very steep leading edge of the output pulse. Figure 4-5 shows the idealized collector and base waveforms.

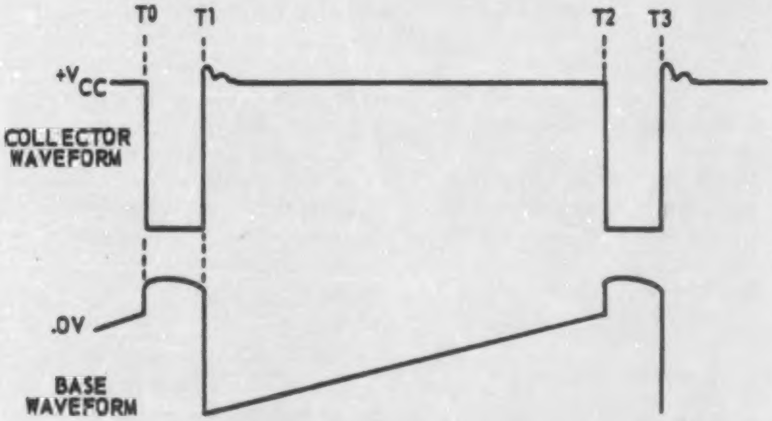

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Figure 4-5. Idealized Waveforms

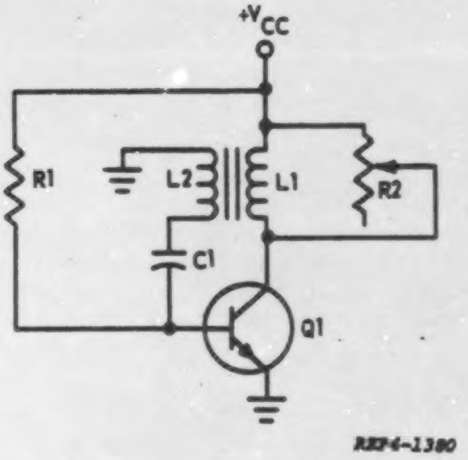

Figure 4-6. Circuit Damping

4-17. Once the base of Q1 becomes saturated the current rise in L1 is determined by the time constant of L1 and the total series resistance. From T0 to T1 in Figure 4-5, the current rise will be approximately linear. The voltage across L1 will be a constant value as long as the current rise through L1 is linear.

4-18. At time T1, L1 saturates. At this time, there is no change in magnetic flux and, thus, no coupling from L1 to L2. C1, which has charged during time T0 to T1, will now discharge through R1 (Figure 4-4). The discharge of C1 will place a negative voltage on the base of Q1 and cut Q1 off. This will cause collector current to stop and the voltage across L1 returns to zero.

4-19. The length of time between T0 and T1 is the pulse width which depends mainly on the characteristics of the transformer, and the point that the transformer saturates. A transformer is chosen that will saturate at about 10 percent of the total circuit current. This insures that the current rise is nearly linear. The transformer controls the pulse width because it controls the slope of collector current rise between points T0 and T1. Since $TC = L/R$, the greater the L, the longer the TC. The longer the time constant, the slower the rate of current rise. When the rate of current rise is slower, the voltage across L1 is constant for a longer time. This primarily determines the pulse width.

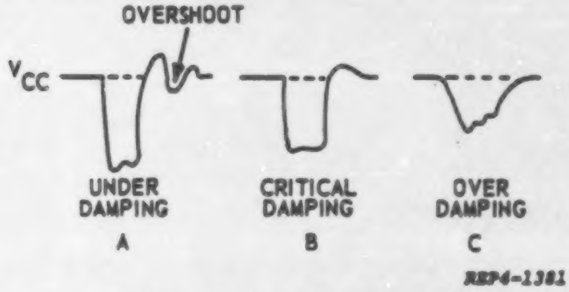

Figure 4-7. Waveform Damping

4-20. From T1 to T2 (Figure 4-5), transistor Q1 is held at cutoff by C1 discharging through R1 (Figure 4-4). The transistor is now said to be "blocked." As C1 gradually loses its charge, the voltage on the base of Q1 gradually returns to a forward bias condition. At T2, the voltage on the base has become sufficiently positive to forward bias Q1, and the cycle repeats.

4-21. The collector waveform may have an inductive overshoot or "parasitic oscillations" at the end of the pulse. When Q1 cuts off, current through L1 ceases, and the magnetic field collapses, inducing a positive voltage at the collector of Q1. These oscillations are not desirable, so some means must be employed to reduce them. The transformer primary may have a high DC resistance, and, thus, a low Q; this will decrease the amplitude of these oscillations. It may be necessary, however, to have more damping than a low Q coil alone can achieve. If so, a swamping or damping resistor can be placed in parallel with L1, as shown in Figure 4-6.

4-22. When an external resistance is placed across a tank, the formula for Q of the tank circuit is $Q = R/X_L$, where R is the equivalent total circuit resistance in parallel with L. You can see from the equation that the Q in figure 4-6 is directly proportional to the damping resistance. Damping resistor R2 is used to adjust the Q and, thus, reduce the amplitude of overshoot or parasitic oscillations. As R2 is varied from infinity toward zero, the decreasing resistance will load the transformer to the point that pulse amplitude, pulse width, and PRF are affected. If reduced enough, the oscillator will cease to function. By varying R2, different degrees of damping can be achieved, three of which are shown in figure 4-7.

4-23. CRITICAL DAMPING gives the most rapid transient response without overshoot. This is accomplished by adjusting R2 to achieve a waveform as shown in figure 4-1B. The resistance will be dependent upon the Q of the transformer. Figure 4-7B shows that oscillations, including the overshoot, are damped out.

4-24. UNDER DAMPING gives rapid transient response with overshoot caused by high or infinite resistance. Figure 4-7A shows underdamping.

4-25. OVER DAMPING is caused by very low resistance and gives a slower transient response and may reduce the pulse amplitude as shown in figure 4-7C.

4-26. The blocking oscillator we have been discussing is a free-running circuit. For a fixed PRF, we need some means of stabilizing the frequency. One method is to apply external synchronization triggers. Refer to figure 4-8. Coupling capacity C2 feeds input synchronization (sync) triggers to the base of Q1.

4-27. If we make the trigger frequency slightly higher than the free-running

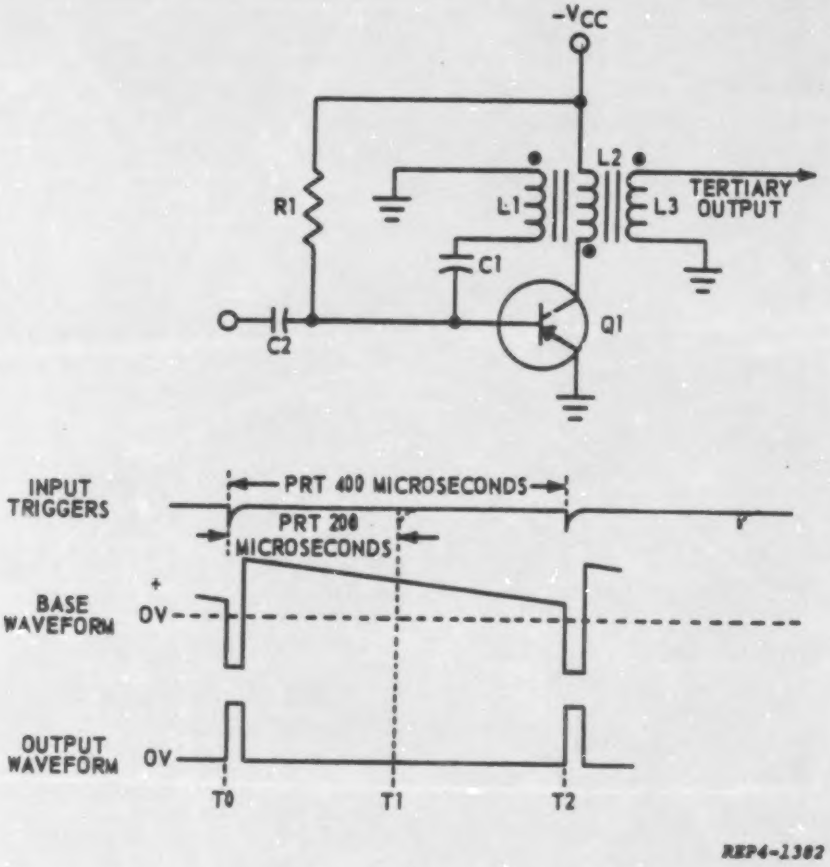
-VCC
L2
R1
L1
L3
TERTIARY OUTPUT
C1
C2
Q1
INPUT TRIGGERS
PRT 400 MICROSECONDS
PRT 200 MICROSECONDS
BASE WAVEFORM
+
OV
OUTPUT WAVEFORM
OV
T0
T1
T2
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Figure 4-8. Synchronized Blocking Oscillator

frequency, the blocking oscillator will "lock in" at the higher frequency. For instance, assume the free-running frequency of this blocking oscillator is 2 kHz, with a PRT of 500 microseconds. If sync pulses with a PRT of 400 microseconds or 2.5 kHz are applied to the base, the blocking oscillator will "lock in" and run at 2.5 kHz. If the sync PRT is too high, frequency division will occur. This means that if the sync PRT is too short, some of the triggers occur when the base is far below cutoff. The blocking oscillator may then synchronize with every second or third sync pulse.

4-28. For example, in Figure 4-8, if trigger pulses are applied every 200 microseconds (5 kHz), the trigger that appears at T1 is not of sufficient amplitude to overcome the cutoff bias and turn Q1 on. At T2, capacitor C1 has nearly discharged and the trigger does cause Q1 to conduct. Note, that with 200 microsecond triggers, the output PRT is 400 microseconds. The output frequency is, thus, one-half the input trigger pulse frequency, and this blocking oscillator becomes a frequency divider.

4-29. Refer to Figure 4-6 for troubleshooting.

Symptom: Parasitic oscillations present at the end of each pulse.

Cause: R2 maladjusted.

Symptom: No output pulse. Collector voltage of Q1 is 0 volts.

Cause: Q1 shorted or L1 open.

Symptom: No output pulse. Collector voltage of Q1 equals V_{CC}.

Cause: Q1 open, or L1 or R2 shorted.

Chapter 5

MULTIVIBRATORS

5-1. Many electronic circuits are not in an "on" condition all of the time. In computers, for example, waveforms must be turned on and off at specific times and for specific lengths of time. The time intervals vary from tenths of microseconds to several thousand microseconds. Square or rectangular waveforms provide the switching action.

5-2. This chapter discusses methods of generating square and rectangular waves, using multivibrators. There are several terms and characteristics of square and rectangular waves that must be discussed prior to the circuitry itself. Let's first review terms you already know; then we will discuss new terms.

5-3. Waveforms

5-4. A waveform which undergoes a pattern of changes, returns to its original value, and repeats the same pattern of changes, is called a periodic waveform. Each completed pattern is called a cycle, and the time for each cycle is called the period of the waveform. The frequency of the waveform is the number of cycles or periods completed in one second.

5-5. Figure 5-1 shows a square wave pattern. A square wave is identified by two alternations, equal in time. The amplitude is measured vertically, and the time of a complete cycle is measured between corresponding points on the wave (T0 to T2, T1 to T3).

5-6. One alternation is often called a "pulse." In this case, the time for one complete cycle is called the pulse recurrence time (PRT). The pulse recurrence frequency (PRF) represents how many times a second the cycle repeats itself. In Figure 5-1, if each alternation were 200 microseconds, the PRT would be 400 microseconds and the PRF would be 2,500 hertz.

$$PRF = \frac{1}{PRT} \quad \text{and } PRT = \frac{1}{PRF}$$

5-7. Figure 5-2 shows a typical rectangular wave. A rectangular wave has two alternations, unequal in time. (Figure 5-2 shows the negative alternation longer than the positive, although this could be the other way around.) If the negative alternation is 300 microseconds and the positive alternation is 100 microseconds, the PRT is 400 microseconds and the PRF is 2,500 hertz.

5-8. Another important part of square and rectangular waves is the "transient interval"

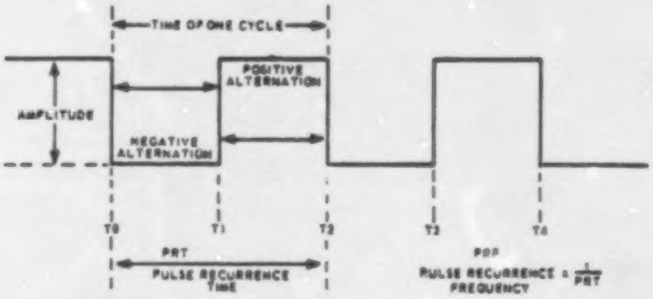

Figure 5-1. Square Waves

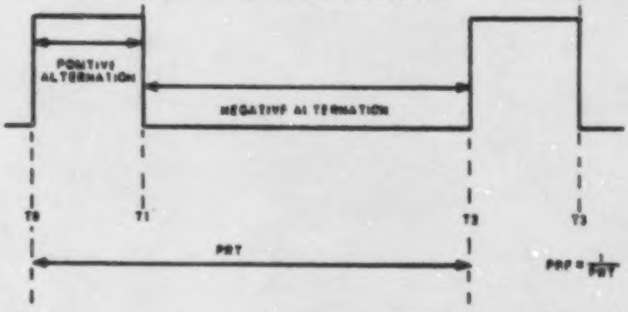
TIME OF ONE CYCLE
POSITIVE ALTERNATION
NEGATIVE ALTERNATION
T0
T1
T2
T3
PRT
PRF = 1/PRT

Figure 5-2. Rectangular Waves

shown in Figure 5-3. It takes time for a voltage or current to change in amplitude. The transient interval is the total time required to go from 0 volts to 100 percent, or from 100 percent of the applied voltage to 0 volts.

5-9. Transient intervals occur on the leading edge of the pulse and on the trailing edge of the pulse.

5-10. Other names used with transient interval are "rise time" and "fall time." Rise time of a waveform is defined as the time required for the voltage to build up from the 10 percent to the 90 percent amplitude point. Fall time is the time required for the voltage to drop from the 90 percent to the 10 percent amplitude point. The rise and fall times of a wave are not necessarily equal. Figure 5-3 shows rise and fall times of 1 microsecond when the total transient interval is 3 microseconds.

5-11. Another term is "pulse width (PW)." This indicates the length of the pulse in time, and is often expressed as the time between the half power points (.707 times pulse

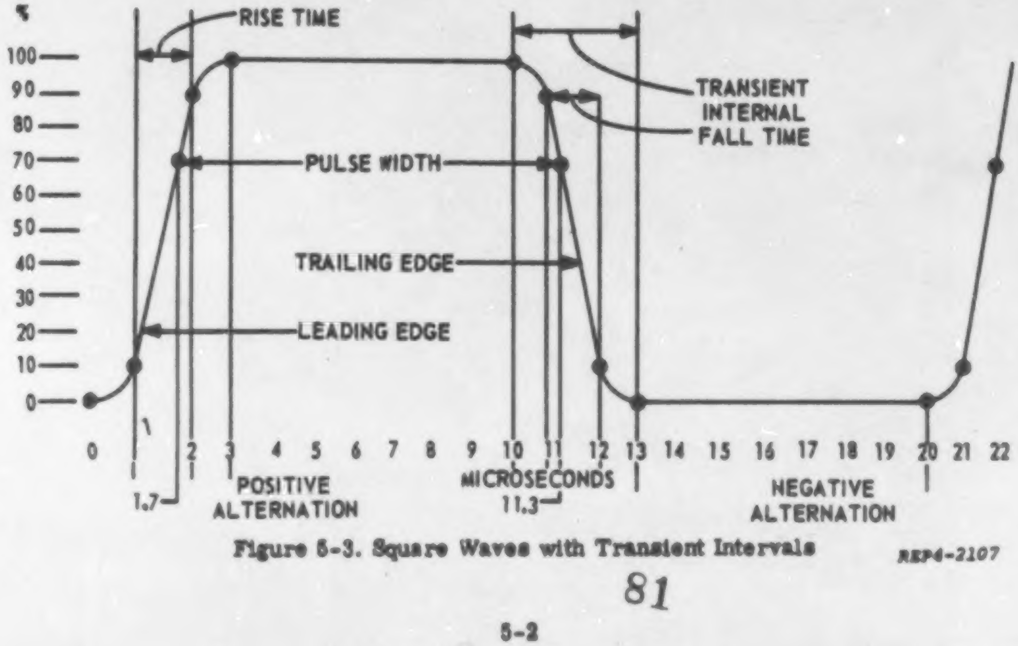
%
100
90
80
70
60
50
40
30
20
10
0
RISE TIME
TRANSIENT
INTERNAL
FALL TIME
PULSE WIDTH
TRAILING EDGE
LEADING EDGE
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
1.7
POSITIVE
ALTERNATION
MICROSECONDS
11.3
NEGATIVE
ALTERNATION

Figure 5-3. Square Waves with Transient Intervals

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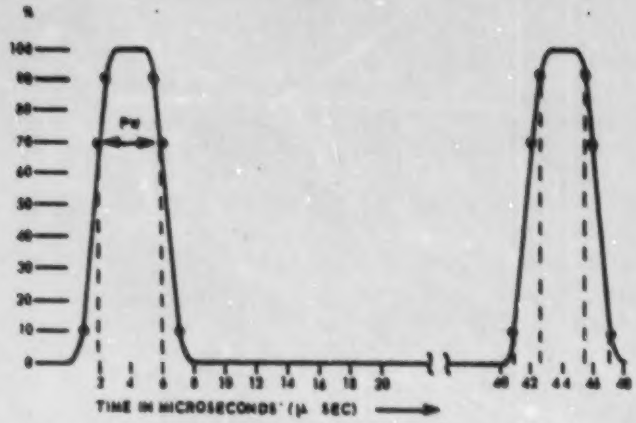


Figure 5-4. Rectangular Waves with Transient Intervals

peak amplitude). Figure 5-3 shows the pulse width, measured at the 70 percent points, as approximately 19.2 microseconds. In computers, pulse width is the time between the two 90 percent amplitude points.

5-12. You may ask, "Why worry about transient interval?" This is a logical question and to answer it, look at Figure 5-4.

5-13. Notice that the PW is 4 microseconds (µsec), and the rise time and fall time make up a large percentage of the pulse time. This is where the transient interval must be considered. The pulse may be as small as a fraction of a microsecond. Waveforms like these should have a very short transient interval. This waveform is usually called a "trigger." A trigger is very narrow, and is normally used to turn circuits on or off.

5-14. Many times a circuit must receive square or rectangular waves; in these cases, the input coupling circuit must pass the wave without distortion. Other times the square or rectangular wave is deliberately distorted. Whether the signal is coupled with or without distortion depends on the coupling circuit.

5-15. Figure 5-5 shows a square wave applied to a series RC circuit. The waveforms for long, medium, and short time constants give a good picture of whether the signal is distorted or not. Let's analyze these waveforms in closer detail.

5-16. With an input square wave that has a PRT of 500 microseconds, each alternation will be 250 microseconds. The time constant

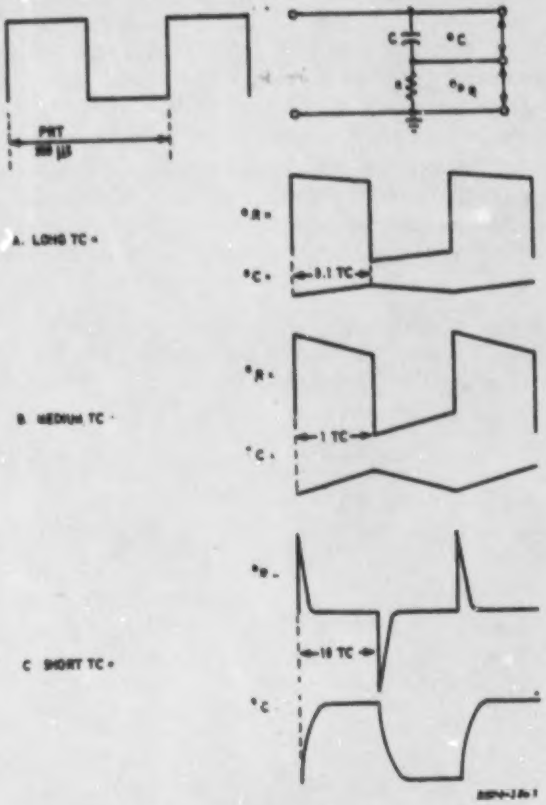


Figure 5-5. Square Wave Applied to a RC Circuit

of R x C (TC = RC) must be greater than 2,500 microseconds to be a long TC. (Recall that a long TC exists when the RC product is 10 or more times the time for one alternation.) For the long TC shown in Figure 5-5A, notice that e_C is very small in amplitude and e_R is approximately the same shape and amplitude as the input signal. An output taken across R, then, has little distortion.

5-17. A medium TC in an RC product that is .1 to 10 times the time for one alternation; in this case, 25 to 2,500 microseconds. Figure 5-5B shows that e_C is larger in amplitude, and e_R is no longer square. An output taken across either component is distorted with respect to the input signal.

5-18. For a short TC, the RC product is .1 (or less) of the time for one alternation. The waveshapes of Figure 5-5C show how e_C resembles the input, but will have rounded corners. The voltage across R is greatly distorted when compared to the input. e_R now resembles a trigger, and it can be used for this purpose. So, by the proper selection of components, a square wave can be coupled to another circuit without distortion, or it can be changed into triggers, whichever is required.

5-19. A series RL circuit can do a similar job. Figure 5-6 shows the circuit with the same square wave input. Figure 5-6A shows a long time constant. Recall TC = $\frac{L}{R}$, and when the time of $\frac{L}{R}$ is 10 or more times one alternation of the wave, we have a long TC. e_L is the undistorted signal and e_R has only a small voltage across it.

5-20. The medium TC of Figure 5-6B has the time of the applied square wave alternation equal to $\frac{L}{R}$. Both e_L and e_R are distorted with respect to the input.

5-21. For a short TC, $\frac{L}{R}$ is one tenth (or less) of the time for one alternation. Figure 5-6C shows the short TC produces a reasonably good square wave across the resistor and a trigger across the coil.

5-22. Multivibrators

5-23. The type of circuit most often used to generate square or rectangular waves is a multivibrator. A multivibrator is basically two amplifier circuits arranged with regenerative feedback. Usually, one of the amplifiers is conducting while the other is cut off.

5-24. When an input signal is large enough, the transistor can be driven into cut off, and its collector voltage will be almost V_{CC}. When the transistor is driven into saturation, its collector voltage will be about zero volts. By designing the circuit to make transistors go quickly from cut off to saturation, a square or rectangular wave can be produced. This principle is used in multivibrators.

5-25. In general, there are three types of multivibrators, according to the number of steady (stable) states of the circuit. (A steady state exists when circuit operation is essentially constant; one transistor remains in conduction and the other remains cut off until an external signal is applied.) The three types of multivibrators are:

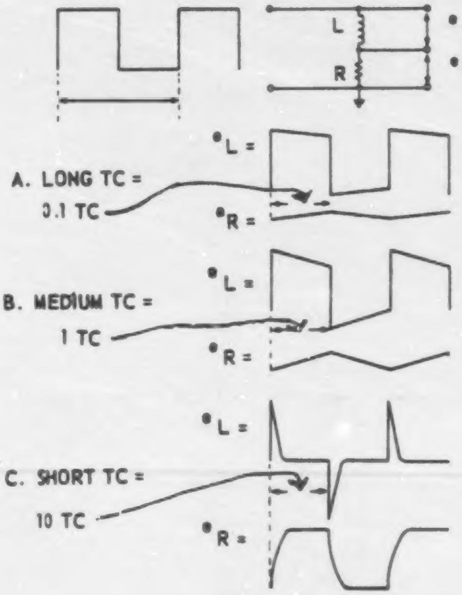


Figure 5-6. Square Wave Applied to a RL Circuit

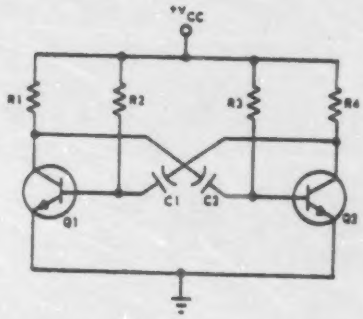


Figure 5-7. Astable Multivibrator

5-26. ASTABLE. This circuit has no stable state. With no external signal applied, the transistors alternately switch from cut off to saturation, at a frequency determined by the RC time constants of the coupling circuits.

5-27. MONOSTABLE. As the name implies, this circuit has one stable state with one transistor conducting and the other cut off. A signal must be applied to change this condition. After a period of time, determined by the internal RC components, the circuit will return to its original condition where it remains until the next signal arrives.

5-28. BISTABLE. This multivibrator has two stable states. It remains in one of the stable states until a trigger is applied, then it goes to the other stable condition to remain there until another trigger is applied to change it back to its first stable state.

5-29. Astable Multivibrator

5-30. The astable multivibrator is used to produce square wave outputs used in gating. Due to relatively unstable frequency, in circuits where accurate timing is necessary, the frequency is stabilized by using an input trigger – of stable frequency – to begin each output square wave. Figure 5-7 shows a collector-coupled astable multivibrator using NPN transistors, connected in a common emitter configuration. The collector voltage of each transistor is coupled back to the base circuit of the other transistor. This provides regenerative feedback. R1 and R4 are the collector load resistors; R2 and R3 provide the forward bias for the transistors; and C1 and C2 are the coupling capacitors. Assume that Q1 = Q2, R1 = R4, R2 = R3 and C1 = C2.

5-31. When V_{CC} is applied, both transistors will conduct. Current will flow through the load resistors, R1 and R4, and the collector voltage on each transistor will drop to some value below V_{CC}. Since no two circuits can be exactly balanced, assume Q1 conducts harder than Q2, causing the collector voltage of Q1 to decrease. C2, as it discharges through R3, couples this negative-going signal to the base of Q2. This negative voltage will cause Q2 to cut off, and the collector voltage of Q2 will increase to V_{CC}. C1 charges to V_{CC} through the forward biased junction of Q1. Q1 is now saturated and Q2 is cut off. This condition continues until C2 discharges enough to permit the emitter-base junction of Q2 to become forward Biased. When Q2 starts to conduct, its collector voltage decreases, causing C1 to discharge through R2. Discharging C1 couples a negative-going signal to the base of Q1, causing it to cut off. As Q1 cuts off, its collector voltage increases toward V_{CC} and C2 charges to this value. Now, Q1 is cut off and Q2 is conducting at saturation. The circuit remains in this state until C1 discharges enough to permit Q1 to conduct, and the cycle repeats.

5-32. Figure 5-8 shows the waveshapes for Figure 5-7. Note, that when the collector

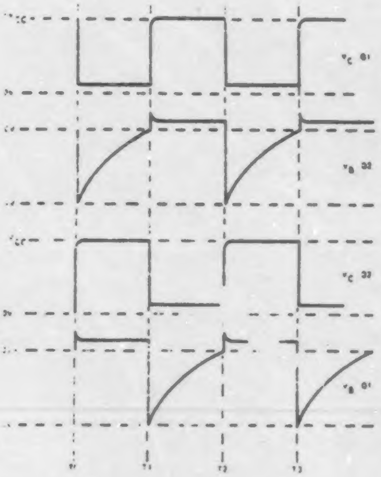


Figure 5-8. Astable Multivibrator Waveshapes

voltage of Q1 is near 0 volts, the collector voltage of Q2 is at V_{CC}. These waveshapes indicate that Q1 is saturated ("on" condition) and Q2 is cut off ("off" condition) from T0 to T1. The opposite conditions are shown between T1 and T2 (Q1 "off" and Q2 "on"). Refer once again to time T0-T1 and note that while Q2 is cut off (collector voltage at V_{CC}), the base waveshape for Q2 (V_{BQ2}) indicates a negative signal, going toward 0 volts. This waveshape is a result of C2 discharging through R3, placing a negative signal on the base of Q2. Also, the base voltage of Q1 (T0-T1) indicates a positive voltage which is enough to keep it saturated. At T1, Q2 conducts, causing C1 to discharge, resulting in a negative voltage on the base of Q1 (V_{BQ1}). This action causes Q1 to cut off. From T1 to T2, Q1 is cut off and Q2 in conducting. The circuit remains in this conduction until C1 discharges enough to allow Q1 to conduct, at T2. Note that the collector voltage of Q1 does not go immediately to V_{CC} when it is cut off. The rounded portion of the waveshape is caused by C2 charging to V_{CC}. Therefore, the coupling capacitors affect the high frequency response of the circuit.

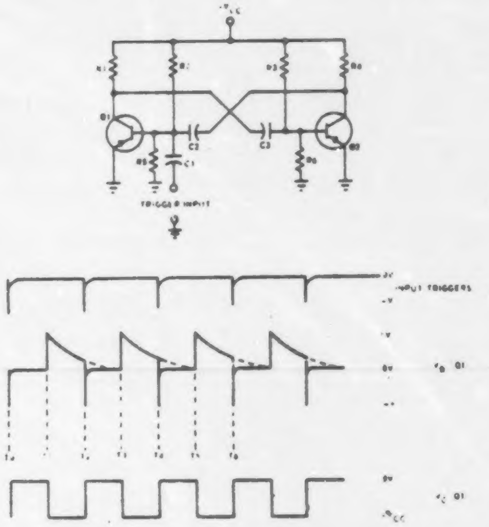


Figure 5-9. Triggered Astable Multivibrator

5-33. The primary factors affecting the PRF and PRT of the circuits are the coupling components. The time each transistor is cut off depends on its time constant: C1-R2 for Q1 and C2-R3 for Q2. If C1 or R2 is increased, the cutoff time of Q1 is increased.

5-34. Some astable multivibrators must have a high degree of frequency stability. A method of obtaining a greater degree of frequency stability is to apply triggers. Figure 5-9 shows the schematic diagram of a triggered astable multivibrator using PNP transistors. At time T0, the negative input trigger to the base of Q1 causes Q1 to go into saturation, which drives Q2 to cut off. The circuit will remain in this condition as long as the base voltage of Q2 is positive, determined by C3, R3, and R6. Observe the parallel paths for C3 to discharge.

5-35. At time T1, Q2 comes out of cutoff and goes into saturation. Also, Q1 comes out of saturation and is cut off. The base voltage waveform of Q1 (Figure 5-9) shows a positive potential that is holding Q1 cutoff. This voltage would normally hold Q1 cutoff until a point between T2 and T3. However, at time T2, another trigger is applied to the base of Q1, causing it to begin conducting. Q1 goes into saturation and Q2 is cut off. This action repeats each time a trigger is applied (T2, T4, T6).

5-36. The PRT of the input triggers must be shorter than the natural free-running PRT of the astable multivibrator, or the trigger PRF must be slightly higher than the free-running PRF of the circuit. This is to

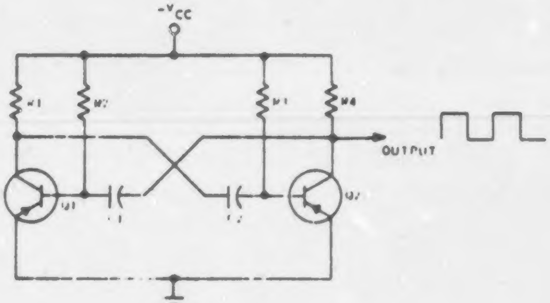


Figure 5-10. Astable Multivibrator (PNP)

make certain the triggers control the PRT of the output.

5-37. Refer to Figure 5-10 for the discussion on troubleshooting. Assume normal operation is free running, with a square wave output obtained from the collector of Q2.

5-38. Symptom: The negative alternation of the output is longer than normal.

Cause: The most logical reason is either R2 or C2 has increased in size.

Symptom: V_C on Q2 is high and V_C on Q1 is very low. This indicates that Q1 is saturated.

Cause: The most likely cause is R3 or Q2 open.

5-39. Monostable Multivibrator

5-40. The monostable multivibrator is a square or rectangular wave generator with one stable condition. With no input signal (quiescent condition), one amplifier conducts and the other is cut off. When an external trigger is applied, the multivibrator will change state for a period of time determined by an RC circuit, and then it will return to its stable state, where it will remain until triggered again. One trigger input causes a full cycle output.

5-41. The monostable multivibrator is used where it is necessary to maintain a constant frequency (PRF), yet have a variable gate output (variable "on" and "off" times). This circuit is frequently used as a "variable gate generator."

5-42. Figure 5-11 shows a monostable multivibrator circuit with its output waveshape. When power is applied to the circuit, Q2 will conduct and Q1 will be cut off.

5-43. Confirm this by checking the forward bias arrangement for the transistors: The Q2 forward bias is conventional, using R2; the Q1 bias uses voltage - divider network R3-R4-R5, connected between $+V_{CC}$ and $-V_{BB}$. Since the circuit uses a negative V_{BB}, it is possible for the voltage on the base of Q1 to be positive OR negative with respect to the emitter (ground). When Q2 conducts, its collector voltage is near 0 volts; this causes a negative voltage on the base of Q1, holding it at cut off. The stable condition of the circuit is Q1 cutoff and Q2 conducting (T0, Figure 5-11B).

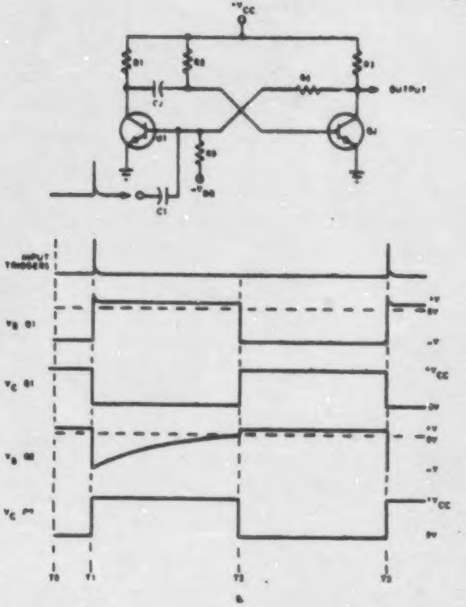


Figure 5-11. Monostable Multivibrator with Waveshapes

5-44. The positive input trigger applied to the base of Q1 causes Q1 to conduct. The collector voltage of Q1 decreases to almost 0 volts, and this negative-going signal is coupled by C2 (discharging through R2) to the base of Q2, which cuts Q2 off. The collector voltage of Q2 now increases toward $+V_{CC}$. Now, voltage divider R3-R4-R5 conduction results in the base of Q1 being positive with respect to its emitter. This voltage keeps Q1 conducting until C2 discharges enough to allow Q2 to conduct once again (T2, Figure 5-11B). When Q2 conducts, its collector voltage decreases, and the base of Q1 becomes negative, resulting in Q1 being cut off. The circuit is again in its quiescent condition, and it will remain there until

78

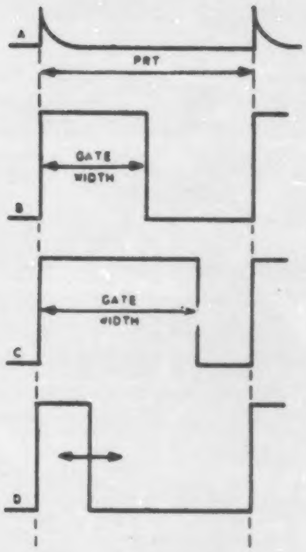


Figure 5-12. Monostable Multivibrator Waveforms with Variable Gate

another trigger is applied (T3, Figure 5-11B).

5-45. The output frequency is controlled by the input trigger frequency. Internally, the point at which the circuit returns to the stable state determines the gate width; this is controlled by the RC time constant of C2 and R2. Figure 5-12 shows the relationship between the trigger and output signal. Part A shows the input triggers; parts B and C illustrate different gate widths. Notice that, while the duration of the gate is different, the duration of the complete cycle is the same as the trigger PRT. Part D of Figure 5-12 indicates that the trailing edge of the positive alternation is variable.

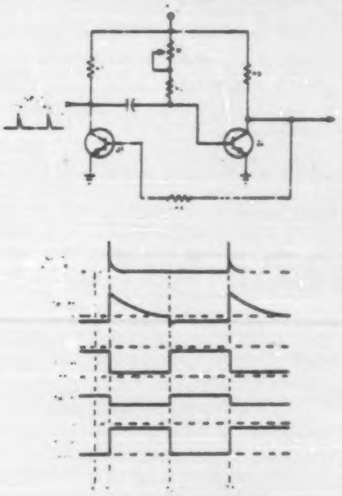


Figure 5-13. Monostable Multivibrator with Waveshapes

5-46. Another version of the monostable multivibrator is shown in Figure 5-13. In its stable condition (at T0), Q1 is cut off and Q2 is conducting. The input trigger (positive pulse at T1), applied to the collector of Q1 and coupled by C1 to the base of Q2, cuts Q2 off, and the collector voltage of Q2 will go toward $-V_{CC}$. The more negative voltage at the collector of Q2 will forward bias Q1, and collector voltage of Q1 will go to about 0 volts. C1 will now discharge and keep Q2 cut off. Q2 remains cut off until C1 discharges enough to allow Q2 to conduct again (T2). When Q2 conducts again, its collector voltage will go toward 0 volts and Q1 will be cut off. Thus, the circuit returns to its quiescent state and has completed a cycle. The circuit will remain in this stable state until the next trigger arrives (T3).

5-47. Note that R3 is variable to allow adjustment of the gate width. Increasing R3 increases the discharge time for C1 which increases the cutoff time for Q2. Making R3 larger, therefore, widens the gate. To decrease the gate width, decrease R3.

5-48. The following symptoms will be caused by the component listed. Use Figure 5-13.

No output waveshape V_C Q1 High V_C Q2 Low	No input triggers, C1 open Q1 open, R4 open R5 open, or R1 short.
No output waveshape V_C Q1 Low V_C Q2 High	R2 open, R3 open, Q2 open, or R5 short.
No output waveshape V_C Q1 Low V_C Q2 Low	R1 open, C1 short, or Q1 short.

87

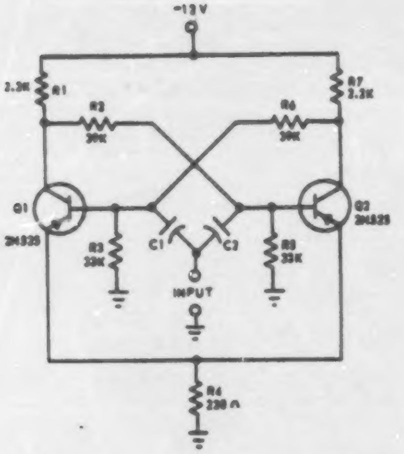


Figure 5-14. Bistable Multivibrator with Circuit Values Indicated

5-49. Bistable Multivibrator

5-50. The bistable circuit, as the name implies, has two stable states. If a trigger of the correct polarity and amplitude is applied, the circuit will change state and remain there until triggered again. The trigger need not have fixed PRF; in fact, triggers from different sources, occurring at different times, can be used to switch this circuit. The bistable multivibrator is used extensively as a counter and storage register in digital equipment.

5-51. The bistable multivibrator circuit is shown in Figure 5-14. In this circuit *R*1 and *R*7 are the collector load resistors. Voltage dividers *R*1-*R*2-*R*5 and *R*7-*R*6-*R*3 provide forward bias for Q2 and Q1 and also couple the collector signal from one transistor to the base of the other. Observe that this is direct coupling of the feedback. This type of coupling is required because the circuit depends on input triggers for operation and not *RC* time constants inside the circuit. Both transistors use common emitter resistor *R*4 which provides emitter coupling. C1 and C2 couple the input triggers to the transistor bases.

5-52. Notice that the circuit is nearly symmetrical, since each transistor amplifier has the same component values. When power is first applied, the voltage divider networks place a negative voltage at the bases of Q1 and Q2. Both transistors have forward bias and both conduct.

5-53. Due to the slight difference between the two circuits, one transistor will conduct harder than the other. Assume that Q1 conducts harder than Q2. The increased conduction of Q1 causes the collector voltage of Q1 to be less negative (more voltage drop across R1. This decreases the forward bias of Q2 and decreases the conduction of Q2. When Q2 conducts less, its collector voltage goes more negative. The negative-going change at the collector of Q2 is coupled to the base of Q1 and causes Q1 to conduct still harder. This regenerative action continues unil Q2 is cut off and Q1 is saturated. The circuit is then in a stable state and will remain there until a trigger is applied.

5-54. At T0, Figure 5-15, current through Q1 causes a 1V drop across *R*4, which places a -1V potential on the Q2 emitter. The collector of Q1 is at -2V, which is dropped across *R*2 and R5, so that the base of Q2 is -0.9V. With its base at -0.9V and emitter at -1V, Q2 is reverse-biased (cut off). Note the Q2 collector is at 11.7V (0.3V drop across R7) and the Q1 base potential is -1.3V, making a 10.4V drop across *R*6 due to Q1 base-to-emitter current.

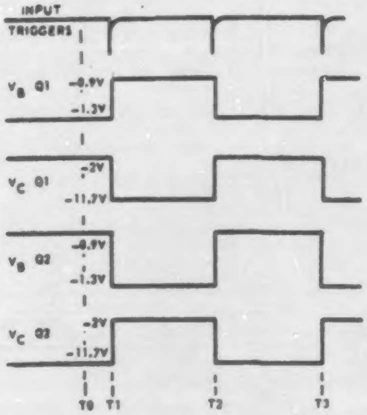


Figure 5-15. Waveshapes for Figure 5-14.

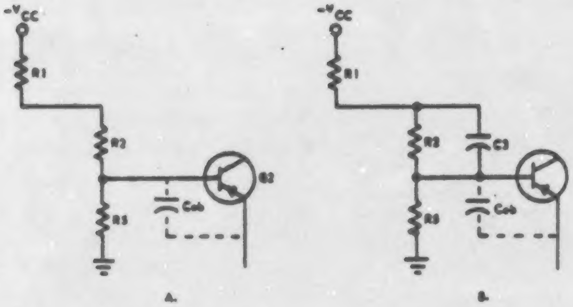


Figure 5-16. High Frequency Compensation Network

5-55. At T1, a negative trigger is applied to both bases through C1 and C2. The trigger does not affect Q1 since it is already conducting. The trigger overcomes cutoff bias on Q2 and causes it to conduct. As Q2 goes into conduction, its collector rises to -2 volts. The positive going change at the Q2 collector causes reverse bias on Q1 and its collector voltage drops to -11.7 volts. The switching action causes a very rapid change of state with Q2 now conducting and Q1 now cut off.

5-56. At T2, a negative trigger is again applied to both bases. This time Q1 is brought into conduction and the regenerative switching action cuts off Q2. The bistable multivibrator will continue to change states as long as triggers are applied. Notice that two input triggers are required to produce one gate; one to turn it on and the other to turn it off. The input trigger frequency is twice the output frequency.

5-57. The transient interval (the time it takes the transistor to go from cut off to saturation, or vice versa) is limited by the interelement capacitance between the base and emitter (C_{eb}). The switching action can be no faster than the time required to charge the interelement capacitance. This leads to rounded corners of the waveforms. It also represents loss of the high frequency components of the square or rectangular waves.

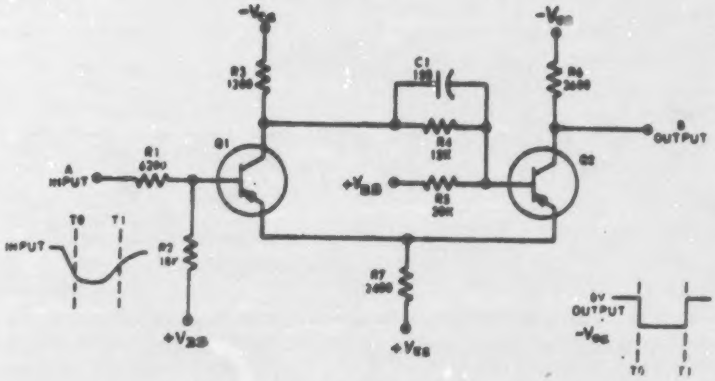


Figure 5-17. Schmitt Trigger

5-58. In Figure 5-16, the base circuit of Q2 (Figure 5-14) is redrawn. The base voltage on Q2 can change only at the rate that C_{eb} charges. To charge C_{eb} current must flow through R1 and R2. This sets up an RC time constant. The load resistor is relatively small (2.2k) and C_{eb} is relatively small (a few picofarads). But R2 is large (39k), which makes the time constant long enough to cause rounding of the corners. This is referred to as "high frequency loss."

5-59. To allow the interelement capacitance to charge faster, the opposition in its charge path must be reduced. A method commonly used is to bypass R2 with a capacitor. Figure 5-16B shows C3 connected across R2. C3 is a low impedance to the high frequency component of the square wave. C3 effectively removes R2 from the circuit during a fast change, and allows C_{eb} to charge faster, reducing the rounded corners of the output waveshape.

5-60. *Refer to Figure 5-14 for troubleshooting.*

Symptom: Positive triggers at the collector of Q1, and negative triggers at the frequency of the input triggers at the collector of Q2.

Cause: R6 open. Q1 will be cut off and Q2 will be conducting. Negative triggers are amplified and inverted by Q1 and cause Q2 to cut off for the duration of the triggers. No gate is produced due to the absence of feedback.

Symptom: Q1 collector to ground measures 0 volts. Positive-going triggers at the collector of Q2.

Cause: Most likely R1 is open. With R1 open, Q1 has no direct path for current flow. The base of Q2 is at ground potential through R5. Negative input triggers cause Q2 to conduct but no feedback occurs.

5-61. SCHMITT TRIGGER

5-62. Usually as a result of the effects of stray capacitance, square and/or rectangular wave signals tend to become rounded on the leading and lagging edges. When this happens, a Schmitt Trigger circuit can be used to restore the signal to its original shape.

5-63. Operational characteristics of the Schmitt Trigger are very similar to the multivibrators you have just studied. However, the few basic differences can be readily seen by observing Figure 5-17.

5-64. Note in this circuit that, like the multivibrators, coupling is provided between the collector of Q1 and base of Q2. However, unlike the multivibrators, no coupling is provided from the collector of Q2 to the base of Q1. But, coupling is provided from Q2 to Q1, and from Q1 to Q2 through common emitter resistor, R7.

5-65. For the present, disregard the input and output signals. Note that the base of Q1 is tied to a positive voltage through R2, and the emitter is tied to a negative voltage caused by the current flowing through Q2 and R7. Therefore, Q1 is reverse biased and cut off. V_CQ1 then, without an input signal, is approximately equal to $-V_{CC}$. Q2, on the other hand, is biased very near (or at) saturation by the current flowing from $-V_{CC}$, through R3, through R4, through the emitter-base junction of Q2, through R7, to $+V_{EE}$. And, V_CQ2 is very near zero volts without an input signal.

5-66. Now, apply the input signal to the base of Q1. Originally, the negative going signal is insufficient to overcome the reverse bias on Q1. However, at T0 of the input signal, the amplitude is sufficient to cause conduction of Q1. Q1 becomes saturated and V_CQ1 very nearly equals zero volts. The combination of change in V_CQ1 and $+V_{BB}$ on the base of Q2, cuts Q2 off; and V_CQ2 very nearly equals $-V_{CC}$.

5-67. At T1 of the input signal, the amplitude is reduced to the point that Q1 again cuts off, and V_CQ1 returns to near $-V_{CC}$. This change is coupled to the base of Q2; Q2 becomes saturated, and V_CQ2 returns to very nearly zero volts.

5-68. C1 in this circuit is for the same purpose as the high frequency compensating capacitors you studied in the Bistable multivibrator. For high frequency changes on the Q1 collector, C1 bypasses R4, and allows these changes to be felt immediately on the base of Q2, thereby preventing "rounding" of the signal we are trying to make square.

5-69. The input and output signals of Figure 5-17 show a fairly accurate picture of what the Schmitt Trigger does. The rounded input signal is changed to a square wave of approximately the same pulse width and PRT.

5-70. Schmitt Trigger circuits are also widely used as voltage-level sensing circuits. When so used, if the input voltage rises above or falls below a specified level, the Schmitt Trigger produces an output; and, the output signal produced would activate a warning device.

5-71. Troubleshooting the Schmitt Trigger circuit is simple if you have mastered amplifier principles and the troubleshooting techniques of other circuits previously studied. However, the following symptoms, causes, and reasons should serve as a good review.

Symptom: No output; V_CQ2 remains very near, or at, zero volts.

Causes: (1) R6 open. All of V_{CC} would be dropped across R6, leaving none to be dropped across Q2.

(2) R3 shorted. In this case, V_CQ1 would remain at $-V_{CC}$, keeping Q2 saturated, and V_CQ2 very nearly equal to zero volts.

(3) R4 or C1 shorted. These two components are in parallel; therefore, if either is shorted, both are shorted. And, with this reduction in resistance between the collector of Q1 and base of Q2, forward bias on Q2 would be increased to the point that the input signal would not cause Q2 to cutoff. There is also a good possibility that this malfunction would cause structure breakdown of Q2.

Symptom: No output; V_CQ2 is at or very near $-V_{CC}$.

Causes (1) R6 shorted. A shorted R6 would drop no voltage, leaving all of $-V_{CC}$ to be dropped across Q2.

(2) R3, R4, or R7 open. With either of these resistors open, there would not be a complete path for forward bias current. Q2 would be cutoff and V_CQ2 would be very nearly equal to $-V_{CC}$.

(3) Q2 open. Applied voltage ($-V_{CC}$ in this case) is dropped across an open component.

Symptom: V_CQ1 remains at or near $-V_{CC}$; V_CQ2 remains at or near zero volts.

Cause: (1) R1 open. Input signal blocked.

(2) Q1 open. Self-explanatory.

(3) R2 shorted. Reverse bias would be too high ($+V_{BB}$ on N type base) for input signal to overcome.

Symptom: High frequency distortion (rounded edges) in output.

Cause: C1 open. Review paragraph 5-67 above for explanation.

Chapter 6

TIME BASE GENERATORS

6-1. Radar sets, oscilloscopes, and computer circuits all use sawtooth (voltage or current) waveforms. Sawtooth waveshapes must have linear rise characteristics. The sawtooth waveform is often used to produce a uniform, progressive movement of an electron beam across the face of an electrostatic cathode ray tube. The movement of the electron beam is called a "sweep." The voltage which causes this movement is a sweep voltage, and the circuit which produces the sawtooth is called a sweep generator, or time base generator. Most common types of time base generators develop the sawtooth waveform with either the charge or discharge of an RC or RL circuit, using some type of switching action.

6-2. Sawtooth Wave

6-3. A sawtooth wave can be generated by the use of an RC network. Possibly the simplest sawtooth generator is that which is shown in Figure 6-1A. Assume that at time T0, S1 is placed in position A. At the first instant, E_a appears across R; C begins to charge toward E_a through R. If S1 remains closed long enough, C will charge to E_a. You remember that it takes 5 time constants for a capacitor to fully charge. In charging the capacitor to the applied voltage, the rate of charge follows an exponential curve. If we desire a linear voltage, we cannot use the full charge of a capacitor.

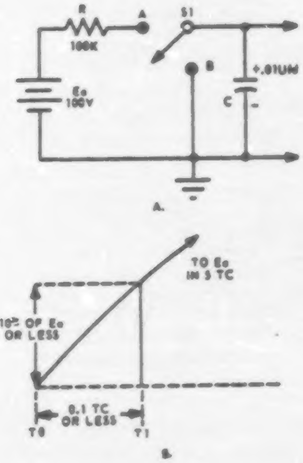


Figure 6-1. Series RC Circuit

6-4. During the first 10 percent of the charge curve, the rate of voltage change across the capacitor is almost constant. In Figure 6-1A, suppose that we place S1 in position A at time T0 and allow C to charge for .1 time constants. This is shown as T0 to T1 in Figure 6-1B. Notice that the rate of voltage change across C is nearly constant between time T0 and T1. Now, assume that at T1 we move the switch from position A to position B. This shorts out the capacitor and it discharges very rapidly. If we place the switch back in position A, the capacitor will start charging again.

6-5. By selecting the size of R and C, we can have a time constant of any value we desire. Further, by controlling the time S1 is left closed, we can have a sawtooth of any duration. In Figure 6-3, if one time constant is 1,000 microseconds, to obtain a reasonably linear sawtooth, S1 should be closed no longer than 100 microseconds. In this example, C1 would charge to nearly 10 volts in .1 time constant.

6-6. There are some special names and terms associated with the sawtooth used in oscilloscopes, so let's define terms before going any further. Figure 6-2 shows a sawtooth

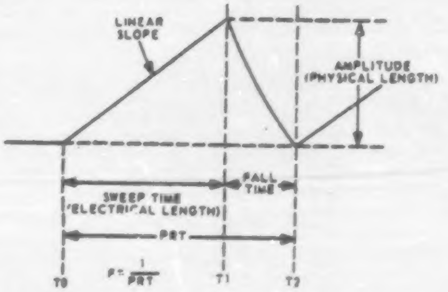


Figure 6-2. Sawtooth

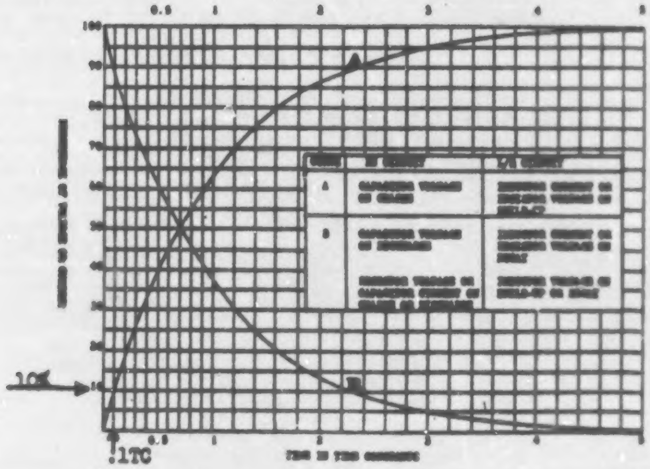


Figure 6-3. Universal Time Constant Chart

waveform with various dimensions labeled. The duration of the rise of voltage (T0 to T1) is called the sweep time or electrical length. It is during this time that the electron beam of an oscilloscope moves across the face of the cathode ray tube. The amount of voltage rise per unit of time is referred to as the slope of the waveform. The time from T1 to T2 is the capacitor discharge time and is called "fall" time or "flyback" time. The reason for the name flyback time is that the electron beam returns or "flies" back to the origin during this time.

6-7. The amplitude of the rise of voltage is called the physical length. It is called physical length because the greater the peak voltage the greater the physical distance the beam will move. For example, it takes twice the voltage to move an electron beam 4 inches as it does to move the beam 2 inches across the face of a given CRT.

6-8. The voltage rise between T0 to T1 is the slope of the wave. The linearity of the rise of voltage is determined by the amount of time the capacitor is allowed to charge. By keeping the time for charge short (10 percent or less of one TC) the linearity is reasonably good.

6-9. In the discussion of time base generators, it was stated that the waveform produced from

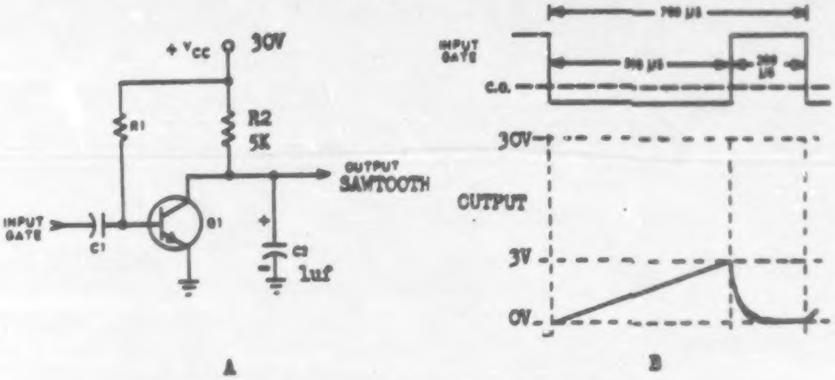


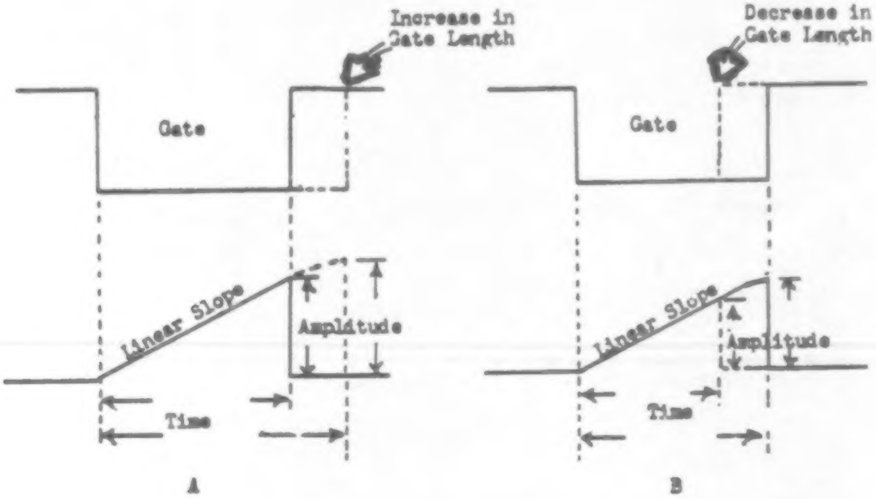
Figure 6-4. Transistor Sawtooth Generator

any sawtooth generator must be LINEAR. A linear sawtooth is one that has an equal change in voltage for an equal change in time. Referring to the Universal Time Constant Chart in Figure 1, we find that the most desirable part of the charge curve is the first one-tenth (.1) of the first TC.

6-10. Referring to figure 6-4A, a Transistor Sawtooth Generator, R1 is a forward biasing resistor for Q1, C1 is a coupling capacitor, Q1 is serving as a switch for the RC network consisting of R2 and C2. With forward bias applied to Q1, it will be conducting at saturation and its collector voltage (the output) will be near zero volts as indicated by the waveform (figure 6-4B). The charge felt by C1 will be near zero. In order to cut Q1 off and allow C2 to charge, a negative gate is applied to the base of Q1. The length of time that the gate is negative will determine how long Q1 will remain cut off and in turn, how long C2 will be allowed to charge. The length of time that C2 is charging is referred to as the ELECTRICAL LENGTH of the sawtooth that is produced.

6-11. The amplitude of the sawtooth that is produced is a direct function of the value of V_{CC} that is used in the circuit. As an example, if the voltage is +30V and the capacitor is allowed to charge to 10% of 30V, then the amplitude of the sawtooth will be 3V (see Figure 6-4). If V_{CC} is increased to 40V, C2 would charge to 10% of 40V and the output would increase in amplitude to 4V. Changing the value of V_{CC} in the circuit will change the amplitude of the sawtooth waveform that is produced, and amplitude determines the PHYSICAL LENGTH. Since the number of time constants used in the circuit has not been changed, LINEARITY will NOT change with a change in V_{CC}.

6-12. The LINEAR slope that is produced by the circuit is dependent on two variables; the time constant (TC) of the RC circuit and the GATE LENGTH of the gate applied to the circuit. For the circuit to produce a LINEAR sawtooth waveshape the components selected should be such that only one-tenth of one TC or less is used. The length of time that the gate is applied to the circuit will control the time that the capacitor is allowed to charge. The value of R2 and C2 will determine the time for one time constant (TC=RC). To determine the number of time constants (or the fraction of one TC) that are used, we divide the time for one time constant into the time that the capacitor is allowed to charge,



Relationship of Gate Length to Linearity or $\#TC = \frac{\text{gate length}}{TC}$. In figure 6-4B, gate length is 500 microseconds and TC is the product of R2 (5k) and C2 (1 uf). The number of time constants $\#TC = \frac{500 \times 10^{-6}}{5 \times 10^{-3}}$ and therefore, $\#TC = .1$.

6-13. Using the formula $\#TC = \frac{\text{gate length}}{TC}$ it is seen that with an increase in gate length, the number of time constants will increase. With an increase in the number of time constants, LINEARITY will decrease. The reason for this is that C2 now charges to a greater percentage of the applied voltage and a portion of the charge curve is being used that is less linear. Observing the waveform in figure 6-5A, we see an increase in amplitude (PHYSICAL LENGTH), an increase in the time that C2 is allowed to charge (ELECTRICAL LENGTH) and a decrease in LINEARITY. If gate length is decreased, figure 6-5B, there is an increase in LINEARITY, a decrease in the time that C2 is allowed to charge (ELECTRICAL LENGTH), and a decrease in amplitude (PHYSICAL LENGTH), as a result of using a smaller percentage of V_{CC}.

6-14. Changing the value of R and C in the circuit affect LINEARITY since they control the time for one time constant. Example: By increasing the value of C2 in the circuit, Figure 6-6A, the time for one time constant would increase and the number of time constants would then decrease. With a decrease in the number of time constants, LINEARITY will increase. The reason for this is that a smaller percentage of V_{CC} is used, and the circuit is operating in a more linear portion of the charge curve. In increasing the value of the TC (C2 or R2), the amplitude of the sawtooth (PHYSICAL LENGTH) decreases because C2 now charges to a smaller percentage of VCC for a given time. ELECTRICAL LENGTH remains the same because we have not changed the length of time that C2 is allowed to charge.

6-15. Decreasing the value of the TC (R2 or C2), figure 6-6B, will result in an increase in the number of time constants and therefore cause LINEARITY to decrease. Anytime there is an increase in the number of time constants, percentage of charge will increase (Universal Time Constant Chart), and amplitude (PHYSICAL LENGTH) will increase. Without an increase in gate length, the time that C2 is allowed to charge through R2 remains the same, therefore ELECTRICAL LENGTH remains the same. LINEARITY will be affected by gate length, the value of R, and the value of C but will not be affected by changing the

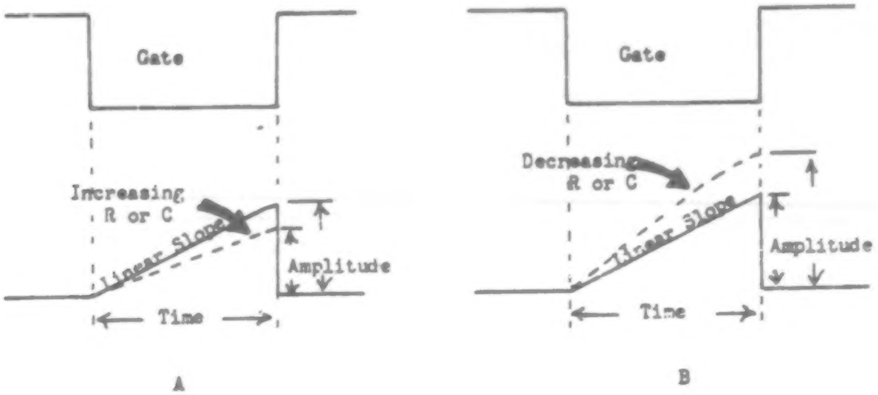


Figure 6-6. Relationship of R and C to Linearity

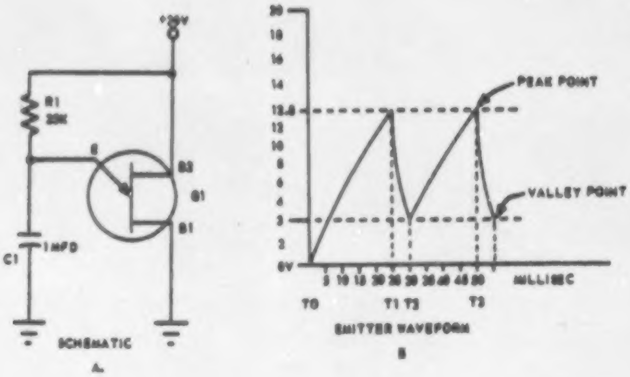


Figure 6-7. Sawtooth Generator

value of V_{CC}. Increasing the gate length will decrease LINEARITY and decreasing gate length will increase LINEARITY. Increasing R or C in the circuit will increase LINEARITY and decreasing R or C in the circuit will decrease LINEARITY.

6-16. The entire time of the sawtooth, from the point where the capacitor begins charging (TO, Figure 6-7) to the point where it starts charging again (T2), is the PRT of the wave. The frequency of the sawtooth wave is equal to one over the time, or $PRF = \frac{1}{PRT}$.

6-17. Unijunction Sawtooth Generator

6-18. So far, we have determined that a switch and an RC network can generate a sawtooth waveform. When using a unijunction transistor as the switch, a simple sawtooth generator looks like the circuit in Figure 6-7A, and the output waveshape like Figure 6-7B.

6-19. When the plus 20 volts is applied across B2 and B1, the voltage distributes evenly, and a voltage of 12.8 volts appears at the N type bar near the emitter. At the first instant, C1 has no voltage across it so the output of the circuit, which is taken across the capacitor, is equal to zero. The voltage across C1 is also the voltage that is applied to the emitter of the unijunction. The unijunction is now reverse biased. After time T0, C1 begins to charge toward 20 volts.

6-20. At time T1, the voltage across the capacitor (the voltage on the emitter) has reached about 12.8 volts. This is the peak point for the unijunction, and it now becomes forward biased. With the emitter forward biased, the impedance between emitter and B1 is now just a few ohms. This is similar to placing a short across the capacitor. The capacitor discharges very rapidly through the low resistance of B1 to E.

6-21. As C1 discharges, its voltage decreases and the voltage from emitter to B1 also decreases. Q1 will continue to be forward biased as long as the voltage across C1 is larger than the valley point of the unijunction.

6-22. At time T2 the 3-volt valley point of the unijunction has been reached. Now, the emitter becomes reverse biased and the impedance from emitter to B1 returns to a high value. Immediately after time T2, Q1 is reverse biased and the capacitor has a charge of approximately 3 volts. C1 will now start to charge toward 20 volt as it did originally. This is shown from T2 to T3 in Figure 6-7B.

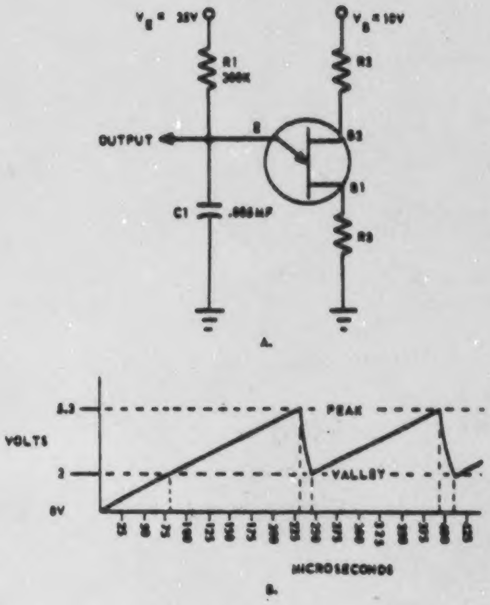


Figure 6-8. Improved Sawtooth Generator

6-23. The circuit operation from now on is just a continuous repetition of the actions between T2 and T3. The capacitor charges until the emitter becomes forward biased, then the unijunction conducts and C1 discharges, then Q1 becomes reverse biased and C1 again starts charging.

6-24. Now, let's determine the linearity, electrical length, and amplitude of the output waveform. First, the linearity: If C1 were allowed to charge to the full 20 volts, it would take 5 time constants (R x C x 5). In the circuit in Figure 6-7B. C1 is allowed to charge from T2 to T3. To find the percentage of charge, use the equation:

$$\frac{\text{E peak} - \text{E valley}}{E_a - E_{\text{valley}}} \times 100 =$$

$$\frac{12.8 - 3}{20 - 3} \times 100 =$$

$$\frac{9.8}{17} \times 100$$

This works out to be about 57 percent. This is far beyond the 10 percent required for a linear sweep voltage. Our linearity is very poor in this example.

6-25. The electrical length (sweep time), which is measured from T2 to T3, can be found by multiplying R x C x the number of time constants. Refer to a Universal Time Constant Chart to find that 57 percent is .83 TC. Multiplying .83 x R1 x C1 you will find that the electrical length is about 20 milliseconds.

6-26. The physical length (amplitude) is determined by subtracting the valley point from the peak point. This is 9.8 volts in our example.

6-27. For a sweep generator that produces a more linear output sawtooth waveform, refer to the circuit in Figure 6-8A. R1 and C1 form the RC time constant. Notice that the capacitor charges toward 35 volts in this circuit.

6-28. The output waveform is shown in Figure 6-8B. With a lower voltage applied from BASE 1 to BASE 2, the peak and valley points are closer together. Calculating the percentage of charge:

$$\frac{E_p - E_v}{E_a - E_v} \times 100 =$$

$$\frac{5.3 - 2}{35 - 2} \times 100 =$$

$$\frac{3.3}{33} \times 100 = 10\%$$

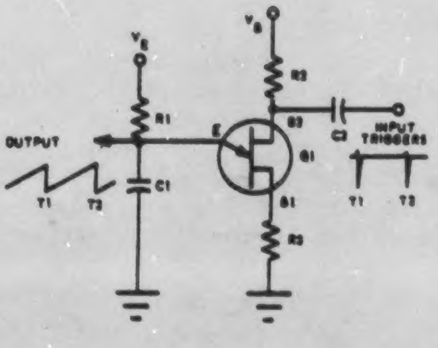


Figure 6-9. Synchronized Sawtooth Generator

Linearity is good. Using a Universal Time Constant Chart, 10 percent charge amounts to .1 time constant. The electrical length is, again, R x C times the number of time constants. With R1 being 300k ohms and C1 being .005 microfarad, the time constant is 1500 microseconds. One tenth of a time constant is equal to 150 microseconds, so the electrical length is 150 microseconds. PRT is the electrical length plus the fall or flyback time. If it takes 15 microseconds for C1 to discharge from 5.3 volts to 2 volts, PRT is 150 + 15, or 165 microseconds. The frequency is $\frac{1}{PRT}$ or about 6 kHz.

6-29. To obtain a very stable PRF some unijunction circuits are triggered. One method is to apply triggers to BASE 2; see Figure 6-5. Negative triggers applied to B2 reduce the interbase voltage enough to cause a forward bias condition in the emitter circuit. This cuts off the sweep and allows C1 to discharge through the B1-to-emitter circuit. Then, C1 recharges until the next trigger arrives, and C1 discharges.

6-30. Transistor Sawtooth Generator

6-31. Our next sawtooth generator uses a conventional PNP transistor, see figure 6-10. We still use an RC network, and the transistor provides the switching action.

6-32. The waveforms for the circuit are shown in figure 6-10B and C. With no input signals, Q1 is biased near saturation by R1. The voltage across C1 is very low (-2.5 volts) because load resistor R3 drops most of the applied voltage. The transistor must be cut off to allow C1 to charge. To cut Q1 off, we use a positive rectangular wave.

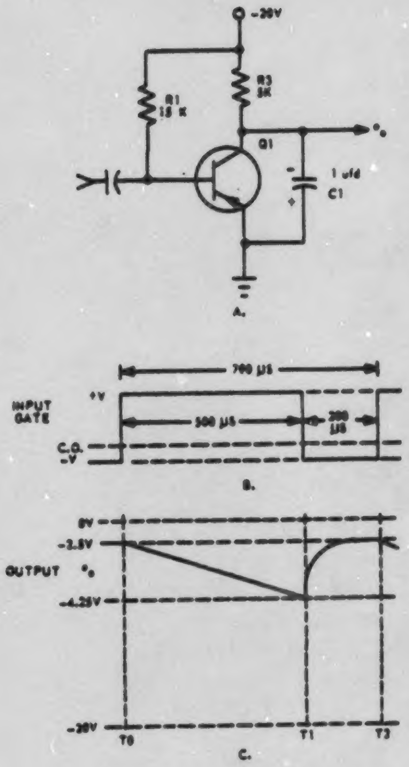


Figure 6-10. Transistor Sawtooth Generator

6-33. Since Q1 is a PNP transistor, a positive voltage must be used to drive it to cutoff. Figure 6-10B shows a rectangular wave input, 500 microseconds long on the positive alternation and 200 microseconds long on the negative alternation. At time T0, the positive gate applied to the base of Q1 cuts Q1 off. This effectively removes the transistor from the circuit (opens the switch), and C1 charges through R3 toward 20 volts. Starting with a charge of -2.5 volts at time T0, C1 charges (T0 to T1) for 500 microseconds to -4.25 volts at time T1. Let's determine the percent of charge:

$$\frac{E_C \max - E_C \min}{V_{CC} - E_C \min} \times 100 =$$

$$\frac{4.25 - 2.5}{20 - 2.5} \times 100 =$$

$$\frac{1.75}{17.5} \times 100 = 10\%$$

This, then, is nearly a linear rise of voltage across C1.

6-34. Increasing the value of R3 or C1 will increase the time constant. The capacitor will not charge to as high a voltage in the same period of time. Decreasing the width of the

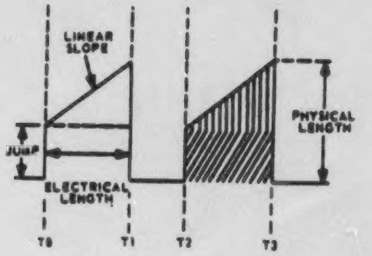


Figure 6-10. Trapezoidal Waveform

gate, and maintaining the same time constant, will also prevent the capacitor from charging as much. With less charge on the capacitor, and the same voltage applied, linearity has been improved. Decreasing R3, C1, or increasing gate width will decrease linearity. Changing the applied voltage will change the charge on the capacitor. The percentage of charge will remain constant; however, not affecting linearity.

6-35. At time T1, the positive alternation of the input gate ends, and Q1 returns to a forward bias condition. A transistor that is near saturation has very low resistance, so C1 discharges rapidly between T1 and T2, see figure 6-10C. The capacitor discharges in less time than 200 microseconds, the length of the negative alternation of the gate. To insure that the circuit has returned to its original condition, the negative gate is made longer than the capacitor's discharge time.

6-36. From time T1 to T2, the capacitor discharges and the circuit returns to its original condition, ready for another positive gate to arrive. The next positive gate arrives at T2 and the actions repeat.

6-37. The amplitude of the output sawtooth wave is equal to 1.75 volts (4.25 volts minus 2.5 volts). The electrical length is the same as the positive alternation of the input gate, or 500 microseconds. The PRT is 700 microseconds (500 + 200) and the PRF is $\frac{1}{PRT}$ or 1,428 hertz.

6-38. Trapezoidal Sweep Generators

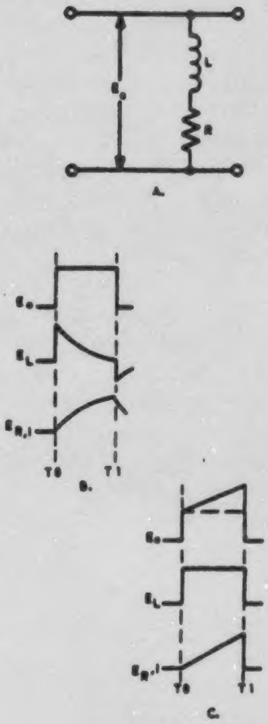


Figure 6-12. Series LR Circuit

Normally, oscilloscopes and synchroscopes use "electrostatic deflection" and, as the name implies, electrostatic fields move the electron beam. The need here is for a sawtooth voltage waveform.

6-39. Another method of electron beam deflection is "electro-magnetic deflection." Currents through a coil produce electromagnetic fields, which position the beam of electrons. The electromagnetic system requires a sawtooth of current. Current must increase at a linear rate. Because of the inherent characteristics of a coil, a sawtooth of voltage does not cause a linear rise of current. A linear rise of current requires a TRAPEZOID voltage waveform applied to a coil. This section discusses the generation of a trapezoidal wave.

6-40. Figure 6-11 shows a trapezoid wave. The wave consists of a sharp, almost instantaneous, jump in voltage followed by a linear rise to some peak value. The initial change in voltage at time T0 is called a "jump" or "step." The jump is followed by a linear sawtooth voltage rise. The time from the jump to the point where the peak value occurs is the electrical length. The peak amplitude is the sum of the jump voltage and the sawtooth peak voltage. The waveshape can be considered a combination of a rectangular wave and a sawtooth wave.

6-41. The inductance and resistance of a coil form a series RL circuit. The voltage drop across this inductance and resistance must be added to obtain the voltage waveform required to produce a linear rise in current. A linear rise of current produces a linear rise of voltage across the resistance of the coil, and a constant voltage drop across the inductance of the coil.

6-42. Assume figure 6-12A represents deflection coils. If we apply a voltage waveshape to the circuit which will provide a square wave across inductor L and a sawtooth across resistor R, then a linear current rise will result.

6-43. Part B of figure 6-12 shows the waveforms when E_a is a square wave. Recall that the inductor acts as an open at the first instant. Current now starts to flow and develops a voltage across the resistor. With a square wave applied, the voltage across the inductor would start to drop as soon as any voltage appears across the resistor. This is due to the fact that the voltage across the inductor and resistor must add up to the applied voltage.

6-44. With E_a being a trapezoidal voltage, Figure 6-12C, the instant current flows and a voltage appears across the resistor, the applied voltage increases. With an increasing applied voltage, the inductor voltage remains constant (E_L) at the jump level and circuit current (E_R, I) will rise at a linear rate from the jump voltage point. Notice that if you add the inductor voltage (E_L) and resistor voltage (E_R) at any point between time T0 and T1, the sum is the applied voltage. The key fact here is that a trapezoid of voltage must be applied to a sweep coil to cause a LINEAR RISE OF CURRENT. The linear rise of current will cause a uniformly changing magnetic field which, in turn, will cause an electron beam to move at a constant rate across a CRT.

6-45. There are many ways to generate a trapezoidal waveshape. For example, the rectangular part could be generated in one circuit, the sawtooth portion in another and the two combined in still a third circuit. A far easier and less complex way is to use an RC circuit in combination with a transistor to generate the trapezoidal waveshape in one stage.

6-46. Figure 6-13A shows the schematic diagram of a trapezoid generator, and the waveshapes for the circuit are in figure 6-13B, R1 provides forward bias for Q1 and, without an input gate, Q1 conducts very hard (near saturation). C1 couples the input gate signal to the base of Q1. R2, R3, and C2 form the RC network which forms the trapezoid wave. The output is taken across R3 and C2.

6-47. With Q1 conducting very hard, collector voltage is near zero volts prior to the gate being applied. The voltage across R2 is about 50 volts which means there is no voltage across R3 and no charge on C2.

6-48. At time T0, the negative alternation of the input gate is applied to the base of Q1, driving it into cutoff. At this time the transistor is effectively removed from the circuit. The circuit is now a series RC network with 50 volts applied. At the instant Q1 cuts off, therefore, 50 volts will appear across the combination of R2 and R3 (the capacitor being a short at the first instant). The 50 volts will divide proportionally, according to the size of the two resistors. R2, then, will have 49.5 volts and R3 will have 0.5 volts. The 0.5 volts across R3, the jump resistor, is the amplitude of the jump voltage. Since the output is taken across R3 and C2 in series, the output "jumps" to 0.5 volts.

6-49. Observe how a trapezoidal generator differs from a sawtooth generator. If the output were taken across the capacitor alone, the output voltage would be zero at the first instant. But, by splitting the R of the RC network so that the output is taken across the capacitor and a part of the total resistance, the jump voltge is produced.

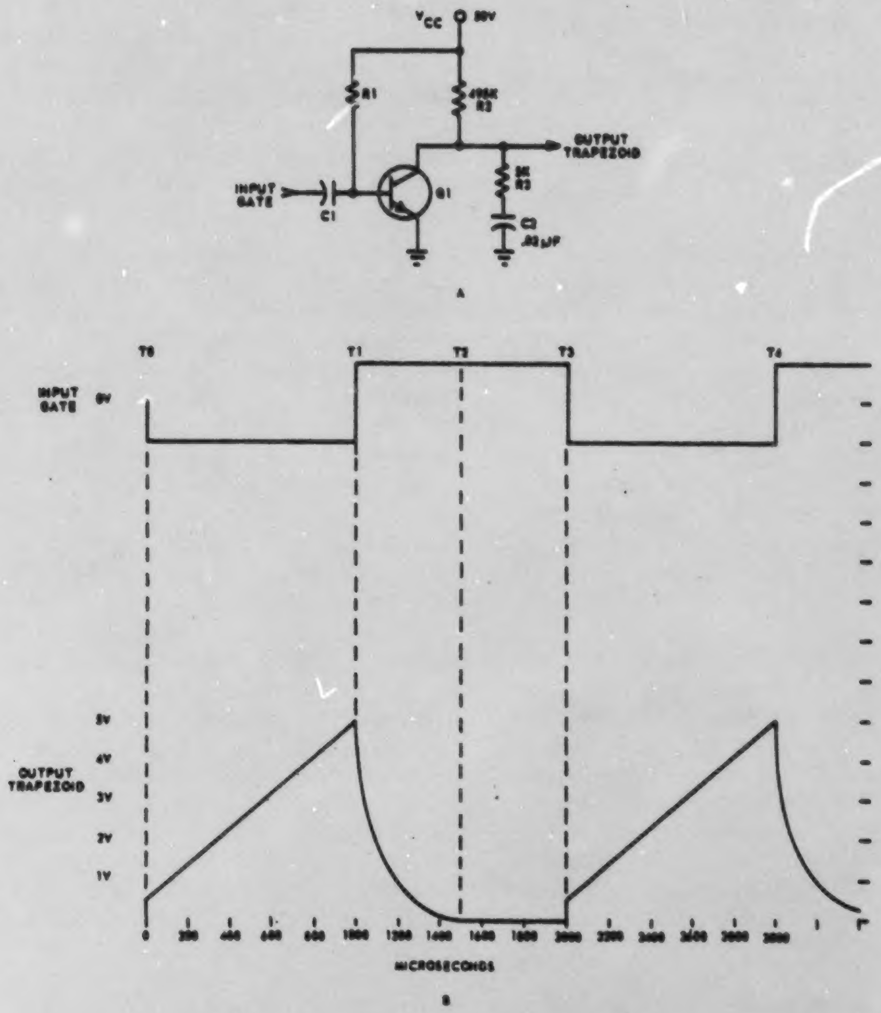

VCC
50V
R1
495K
R2
OUTPUT TRAPEZOID
INPUT GATE
C1
Q1
5K
R3
C2
.02 µF
A
T0
T1
T2
T3
T4
INPUT GATE
0V
5V
4V
3V
2V
1V
OUTPUT TRAPEZOID
0
200
400
600
800
1000
1200
1400
1600
1800
2000
2200
2400
2600
2800
3000
MICROSECONDS
B

Figure 6-13. Trapezoidal Generator

6-50. Referring again to figure 6-13, from T0 to T1, C2 begins charging toward 50 volts through R2 and R3. The time constant for this circuit is 10 milliseconds. If the input gate is 1,000 microseconds, the capacitor can charge for only 10 percent of one TC, and the sawtooth part of the trapezoid wave will be linear.

6-51. At time T1, the input gate ends, and Q1 begins to conduct heavily. C2 discharges through R3 and Q1. The time required to discharge C2 is primarily determined by the values of R3 and C2. The minimum discharge time (in this circuit) is 500 microseconds (5k x .02 µF x 5). At time T2, the capacitor has discharged back to zero volts, and the circuit is quiescent. It remains in this condition until T3 when another gate is applied to the transistor.

6-52. We calculated the amplitude of the jump voltage, which was 0.5 volts. The sawtooth portion of the wave is linear because the time, T0 to T1, is only 10 percent of the total charge time. The amplitude of the trapezoid wave is approximately 5 volts. The electrical length is the same as the input gate length, or

1,000 microseconds. Linearity is affected in the same manner as in the sawtooth generator. Increasing R2, C2, or decreasing gate width will improve linearity. Changing the applied voltage will increase output amplitude, but will not affect linearity.

6-53. Linearity of the trapezoidal waveform, produced by the circuit in figure 6-13 will be dependent on two factors: GATE LENGTH and the TIME CONSTANT (TC) of the RC circuit. Recall that these are the same factors that controlled LINEARITY in the Sawtooth Generator. The formula developed earlier will still remain true and enable us to determine what effect these factors will have on LINEARITY.

$$\#TC = \frac{\text{gate length}}{TC}$$

6-54. An increase in gate length will result in an increase in the number of time constants and an increase in the percentage of charge that the capacitor will take on during this time interval. We stated earlier that if the number of time constants were to exceed .1 that LINEARITY would decrease. The reason for a decrease in LINEARITY is that a greater percentage of V_{CC} is used and from the Universal Time Constant Chart, we can observe that the charge line begins to curve. A decrease in gate length will have the opposite effect on LINEARITY in that it will cause LINEARITY to increase. The reason for this increase is that we are using a smaller number of time constants and in turn, a smaller percentage of the applied V_{CC}.

6-55. Changing the value of resistance or capacitance in the circuit also effects LINEARITY. If the value of C2 or R3 is increased this would increase the time for one time constant. An increase in TC will result in a decrease in the number of time constants (#TC). As stated earlier, a decrease in the #TCs will result in an increase in LINEARITY (less than .1 TC). In addition to an increase in LINEARITY, there would also be an increase in JUMP VOLTAGE (larger value of R3) and a decrease in the amplitude (PHYSICAL LENGTH) of the SAWTOOTH produced by the circuit. ELECTRICAL LENGTH will remain the same as the length of the gate was not changed.

6-56. R-2 will have a similar effect on LINEARITY as it is in series with R3. As an example, decreasing the value of R2 will result in a decrease in LINEARITY. From the equation $\#TC = \frac{\text{gate length}}{TC}$ we find that by decreasing R ($TC = RC$), the #TCs will increase, and an increase in the number of time constants causes a decrease in LINEARITY. Other effects would be an increase in JUMP VOLTAGE and an increase in the amplitude (PHYSICAL LENGTH) of the SAWTOOTH.

6-57. Changing the value of V_{CC} does not affect LINEARITY as linearity is dependent on Gate Length, R and C. V_{CC} will have an effect on the amplitude of the waveform and the value of JUMP VOLTAGE that is obtained.

NOTES

Chapter 7

LIMITERS AND CLAMPERS

7-1. Often the amplitude or the reference level of a signal must be modified as the signal passes from one circuit to another. This chapter explains how limiters and clampers perform these functions.

7-2. Limiters

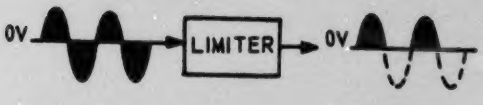
7-3. As an electronic technician you will be confronted with many different types of limiting circuits. They vary in design according to their purpose and use. A thorough knowledge of the principles of limiters is essential.

7-4. A limiter is defined as a device which "limits" or prevents some characteristic of a waveform from exceeding a specified value. This text discusses limiting the amplitude of a waveform, as the removal of one or both peaks of the waveform at a desired level.

7-5. Limiting circuits are used for two primary purposes, (1) waveshaping and (2) protection. Limiters used as waveshaping circuits clip or modify the waveshape of a signal. Limiters used as protective circuits prevent a voltage from exceeding a specified negative or positive reference level.

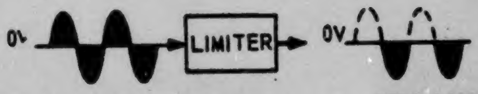
7-6. A limiter which removes a portion of the negative half-cycle of a waveshape is called a "negative" limiter. As an example of negative limiting, notice how the waveshape in Figure 7-1 has been modified.

7-7. Another type of limiting is the "positive limiter" which removes positive amplitudes.



REP4-1441

Figure 7-1. Negative Limiter



REP4-1442

Figure 7-2. Positive Limiter

Figure 7-2 shows positive limiting, removing the positive half-cycle of a waveshape.

7-8. Series Limiters

7-9. A diode will conduct when its anode voltage is positive with respect to its cathode voltage. The diode will not conduct (neglecting reverse current) when the anode is negative with respect to the cathode. Limiters use this principle along with voltage divider action in their operation.

7-10. A block diagram of a series limiter is shown in Figure 7-3. A diode is connected in series with a resistor; the input is applied to the combination, and the output is taken across the resistor. When the diode is forward biased it acts as a short, and the output is approximately the same as the input -- with no limiting. When the diode is reverse biased it acts like an open, no output and limiting occurs.

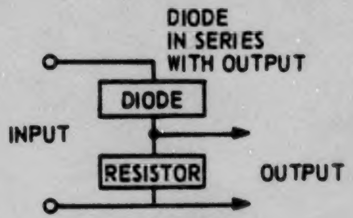


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Figure 7-3. Block Diagram of a Series Limiter

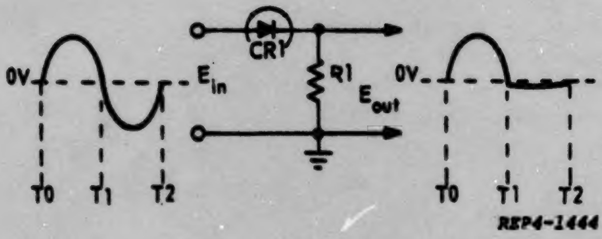


Figure 7-4. Series Negative Limiter

7-11. Figure 7-4 shows the schematic diagram with the input and output waveforms for a SERIES NEGATIVE LIMITER. The key for identification is the diode in series with the input signal. Further, it is a negative limiter because limiting takes place during the negative half-cycle. Let's consider each half-cycle of the input signal and determine how the output is produced. During T0 to T1, the anode is more positive than the cathode and the diode conducts. As current flows up through the resistor and the diode, a positive voltage is developed as the output. During T0 to T1, the voltage across the resistor is essentially the same as the voltage applied to the circuit (neglecting the small voltage that is dropped across the diode).

7-12. During T1 to T2, the anode is negative with respect to the cathode and the diode does not conduct. This portion of the output indicates limiting, because there is no current through the resistor (neglecting the small reverse current).

7-13. The schematic diagram shown in Figure 7-5 is a SERIES POSITIVE LIMITER since the diode is in series with the signal and the positive half-cycle of the waveform is limited. When the positive alternation of the input signal (T0 to T1) is applied to the circuit, the cathode is positive with respect to the anode. The diode is reverse biased and the positive alternation of the input signal is limited. The extremely small output is the result of reverse current flow.

7-14. During T1 and T2 of the input signal the cathode is negative, which forward biases the diode, and current flows through the resistor developing an output. The output on the negative alternation is approximately the same amplitude as the input, so no limiting occurs.

7-15. Ideally, the output waveshape exactly duplicates the input, with the limited portion removed. During the limited portion of the signal the diode resistance should be high; for the unlimited portion of the signal, the resistance of the diode must be small compared to the resistor. Therefore, the diode requires a very high front-to-back ratio (forward resistance compared to reverse

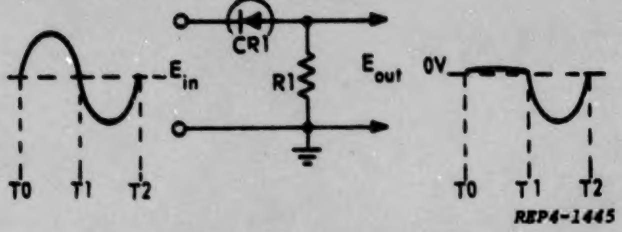


Figure 7-5. Series Positive Limiter

resistance). The following formula can be used to determine the output amplitude of the signal:

$$E_{out} = \frac{R}{R + R_{ac}} E_{in}$$

Where E_{out} is the output amplitude, R is the value of resistor R1, and R_{ac} is the AC resistance of the diode from anode to cathode, and E_{in} is the input signal amplitude.

7-16. To summarize, a series limiter has the output in series with the diode. When the diode conducts, the output resembles the input. When the diode is cutoff, the output is nearly zero. The portion of the input signal which does NOT appear in the output determines whether the limiter is positive or negative. A negative limiter is changed to a positive limiter by reversing the diode connections.

7-17. Shunt Limiters

7-18. A shunt limiter circuit uses the same diode theory and voltage divider action as the series limiter. Figure 7-6 shows the block diagram of a shunt limiter. A resistor and diode are connected in series with the input signal, and the output signal is taken across the diode. The output is in "shunt" with the diode, hence the name, shunt limiter.

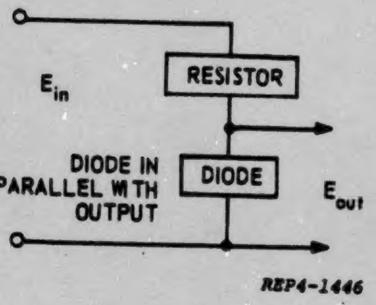


Figure 7-6. Block Diagram of a Shunt Limiter

7-19. The schematic diagram shown in Figure 7-7 is a SHUNT POSITIVE LIMITER since the diode is in shunt with the output and the positive half-cycle of the input is limited. When the positive alternation of the input signal is applied to the circuit (T0 to T1), the diode becomes forward biased and conducts. As current flows up through the diode and the resistor, a voltage is dropped across each. With R1 being much larger than the forward resistance of CR1, most of the input signal is dropped across R1. This leaves only a very small voltage across the diode as the output. The positive alternation of the input signal has been limited.

7-20. During T1 to T2, the diode is reverse biased and acts as an extremely high

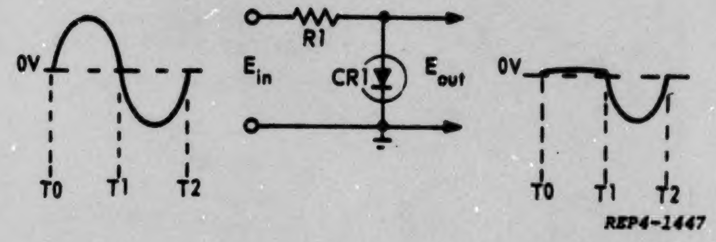
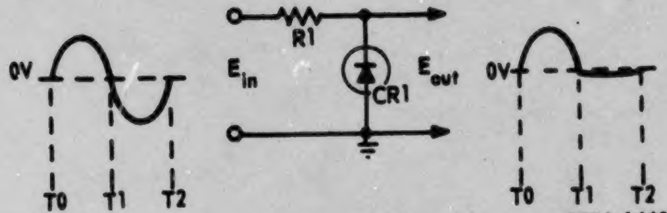


Figure 7-7. Shunt Positive Limiter



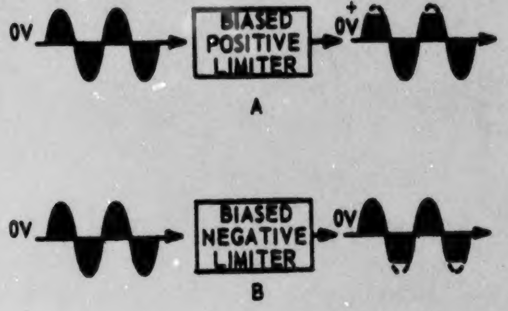
REP4-1448

Figure 7-8. Shunt Negative Limiter

resistance. The negative alternation of the input signal appears across the diode at approximately the same amplitude as the input. The negative alternation of the input signal is not limited.

7-21. Notice the similarity of the shunt positive limiter and the SHUNT NEGATIVE LIMITER shown in Figure 7-8. The diode connections are reversed. From T0 to T1 of the input signal, the diode is reverse biased and does not conduct. The output signal is the input signal slightly reduced in amplitude. The positive alternation is NOT limited.

7-22. During the negative alternation of the input signal, T1 to T2, the diode becomes forward biased and conducts. As current flows through the resistor and diode, a voltage is developed across each. With the series resistor being much larger than the resistance of the diode, most of the input signal appears across R1. This leaves only a small voltage across the output diode, and the negative alternation of the signal is limited.



REP4-1449

Figure 7-9. Biased Shunt Limiters

7-23. As with the series limiter, the shunt limiter should provide maximum output voltage for the unlimited portion of the signal, the diode's reverse-bias resistance must be very large compared to the series resistor. And, to provide minimum output for the limited portion of the signal, the diode's forward-bias resistance must be very small compared to the series resistor. To determine the output amplitude the following formula can be used:

$$E_{out} = \frac{R_{ac}}{R_{ac} + R} \quad E_{in}$$

Where E_{out} is the output signal amplitude, R_{ac} is the AC resistance of the diode, R is the series resistor R1, and E_{in} is the input signal amplitude.

7-24. To summarize, a shunt limiter has the output in shunt with the diode. When the diode conducts, the output voltage is nearly zero, and when the diode is cut off the output is nearly the same as the input voltage.

7-25. Biased Shunt Limiters

7-26. In the shunt limiters discussed thus far, limiting takes place near a zero reference level. Limiting may take place at any

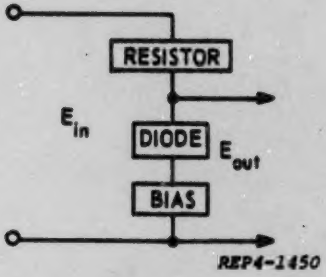


Figure 7-10. Block Diagram of a Biased Shunt Limiter

positive or negative reference level. That is, a limiter may remove only a portion of one alternation. An example of such limiting is illustrated in Figure 7-9. Part A shows only the extreme positive portion of the wave limited and part B shows only the extreme negative portion of the wave limited.

7-27. A block diagram of a biased shunt limiter is shown in Figure 7-10. The resistor, diode, and bias supply are connected in series, and the input signal is applied to this combination. The output from the circuit is taken across the diode and the bias supply together.

7-28. A schematic diagram of a POSITIVE SHUNT LIMITER WITH POSITIVE BIAS is shown in Figure 7-11. Battery B1 is connected with the positive terminal to the cathode of the diode. This causes the diode to be reverse biased at all times except when the input signal is more positive than the bias voltage.

7-29. The relative size of the circuit components are as follows: R_{ac} of the diode in the forward biased direction is 10 ohms, the resistance of the diode in the reverse biased direction is 1 megohm, R1 is 1 k ohm, B1 is 4 volts, and the input signal has a 10-volt peak. As the positive alternation of the input signal is applied (T0 to T1), the output voltage follows the input signal. During time T1 to T2, the input signal is more positive than 4 volts; the diode is forward biased and conducts. At this time, the output voltage equals the bias voltage. Limiting takes place between T1 and T2, and the output is approximately 4 volts. With an increase in bias, limiting would take place at a higher positive voltage, and there would be less limiting of the output signal.

7-30. From T2 to T4 of the input signal, the diode is reverse biased and does not conduct. The output signal follows the input signal and no limting takes place.

7-31. This circuit is called a POSITIVE LIMITER WITH POSITIVE BIAS because limiting takes place in the positive alternation, and positive bias is used on the diode, since the cathode is positive with respect to ground.

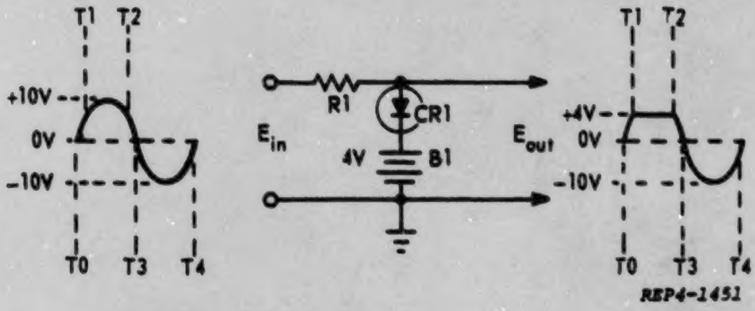


Figure 7-11. Shunt Positive Limiter with Positive Bias

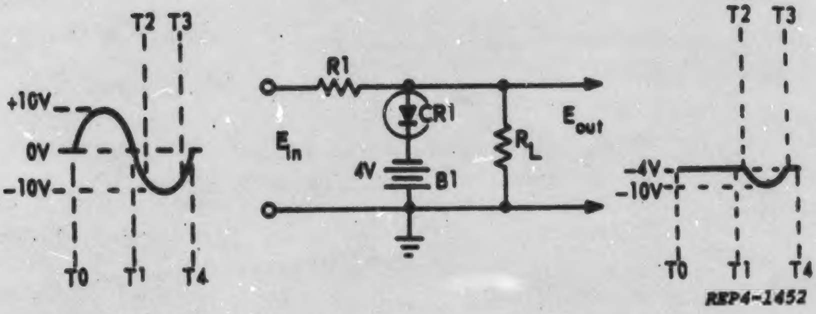


Figure 7-12. Shunt Positive Limiter with Negative Bias

7-32. Figure 7-12 shows the schematic diagram of a SHUNT POSITIVE LIMITER WITH NEGATIVE BIAS. The only difference from Figure 7-11 is the reversed battery. Now, the diode is forward biased and conducts before an input signal is applied. Considering CR1 as a short during conduction, the voltage across the E_{out} terminals is -4 volts.

7-33. As the positive alternation of the input signal is applied to the circuit, the diode remains forward biased and limits the entire positive alternation (T0 to T1). As the signal goes in a negative direction (T1 to T2), the diode is still forward biased and limiting is still present. The only time CR1 becomes reverse biased is when the anode goes more negative than its cathode. When the input signal is more negative than the -4 volts of the bias battery, the diode becomes reverse biased and cuts off. The output follows the input signal from T2 to T3, at all other times, the diode is forward biased and limiting occurs. With an increase in negative bias, the diode conducts for a longer portion of the input signal and more limiting will be present in the output.

7-34. This circuit is called a shunt positive limiter with a negative bias since the positive output is limited, and the bias in the circuit is negative with reference to ground. Limiting takes place at all points more positive than -4 volts.

7-35. The circuit shown in Figure 7-13 is a SHUNT NEGATIVE LIMITER WITH NEGATIVE BIAS. Again, assume the forward-bias resistance of CR1 is 10 ohms, the reverse-bias resistance of CR1 is 1 megohm R1 is 1 k ohm, B1 is -4 volts, and the input peak is 10 volts. With no input, battery B1 reverse biases CR1. CR1 cannot conduct

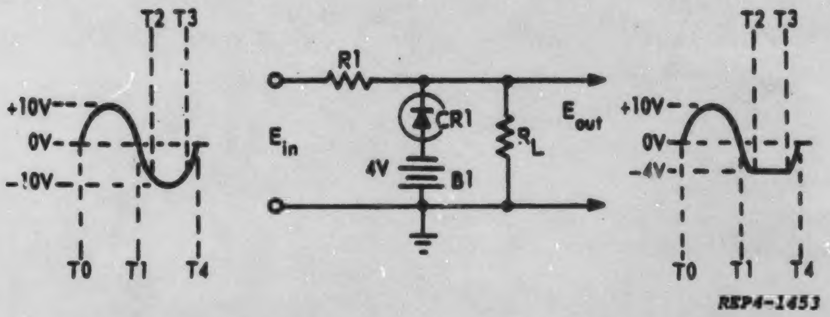


Figure 7-13. Shunt Negative Limiter with Negative Bias

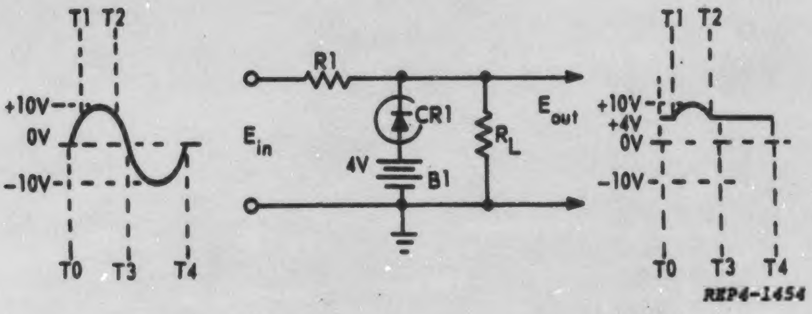

T1 T2
+10V
0V
-10V
T0 T3 T4
R1
CR1
4V
B1
E_in
R_L
E_out
T1 T2
+10V
+4V
0V
-10V
T0 T3 T4
REP4-1454

Figure 7-14. Shunt Negative Limiter with Positive Bias

until its cathode is more negative than its anode. Thus, CR1 acts as an open until E_{in} goes below -4 volts. During the positive alternation of the input of the input signal the output follows the input and no limiting occurs.

7-36. When the input signal becomes negative enough to forward bias the diode, CR1 conducts and acts like a short (10 ohms in series with 1 k ohm). The input signal is developed across R1, and the output signal during time T2 to T3 is -4 volts. If the -4 volts is increased, limiting will take place at the new bias level and less limiting will be present in the output.

7-37. Between T3 and T4, the diode is again reverse biased and the output signal follows the input signal. No limiting occurs.

7-38. A SHUNT NEGATIVE LIMITER WITH POSITIVE BIAS is shown in Figure 7-14. Now, you should be able to determine the output waveform. The operation is similar to those circuits already explained. Limiting occurs when the diode conducts, and there is no limiting when the diode is reverse biased. In this circuit, the bias battery forward biases the diode without an input signal. E_{out} is +4 volts except where the input goes above +4V (T1 to T2). All of the signal which is more negative than +4V is limited. If the +4V is increased, there will be more limiting in the output.

7-39. A DOUBLE DIODE LIMITER (Figure 7-15) uses a shunt positive limiter with positive bias (CR1 and B1) and a shunt negative limiter with negative bias (CR2

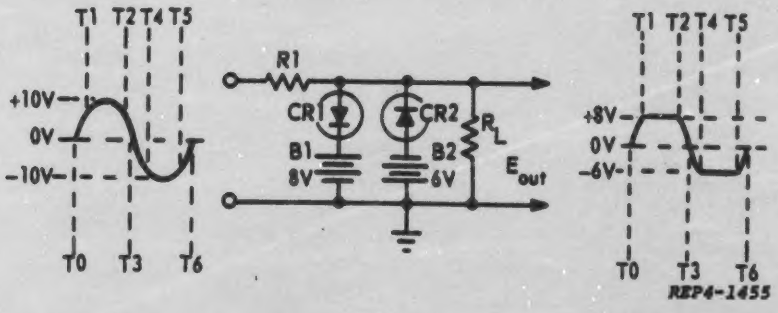

T1 T2 T4 T5
+10V
0V
-10V
T0 T3 T6
R1
CR1
CR2
B1
8V
B2
6V
R_L
E_out
T1 T2 T4 T5
+8V
0V
-6V
T0 T3 T6
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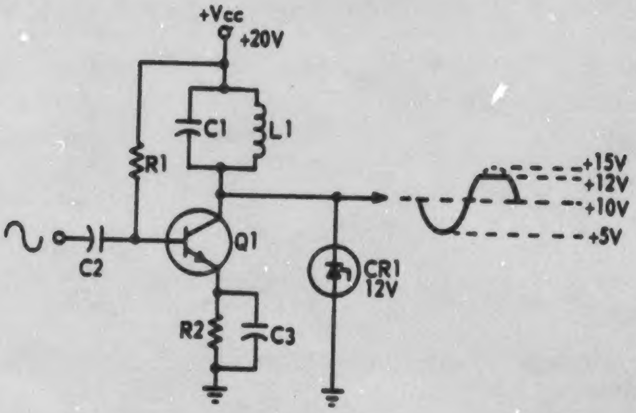
Figure 7-15. Double Diode Limiter



REP4-1456

Figure 7-16. Zener Diode Limiter

and B2). Neither diode is forward biased with no input signal. When the input signal becomes more positive than 8 volts, CR1 conducts and limits the output to this value. When the input signal becomes more negative than 6 volts, CR2 conducts and limits the output to this value. When neither diode conducts, the output follows the input waveform.

7-40. Zener Diode Limiter

7-41. Figure 7-16 shows one example of how a zener diode can be used as a limiter for protection puroses. A common emitter RF amplifier has a zener diode connected from the collector to ground. CR1 is a 12-volt zener diode. Assume that during normal operation the voltage on the collector of Q1 varies between +9 volts and +11 volts. This value of voltage across the zener is not enough to cause zener action, so the diode acts like a large resistance. Due to the input signal and the reactive collector load, collector voltage could become high enough to damage the transistor. (Recall at resonance how the voltage across a reactance equals Q times E_a). However, as the voltage across the zener reaches 12 volts, the diode conducts. Therefore, the voltage on the collector of Q1 cannot exceed 12 volts in this example. This feature is particularly useful when the collector load impedance is reactive. Zener diodes are frequently used to protect against such high voltages.

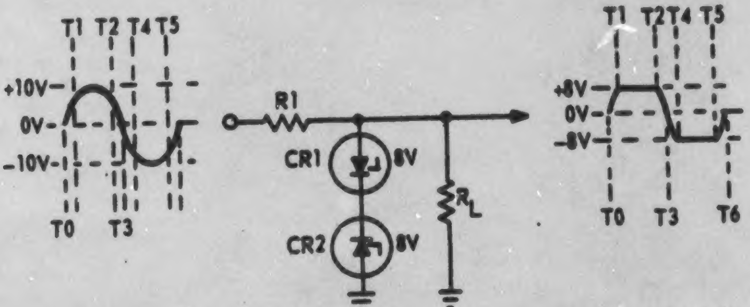


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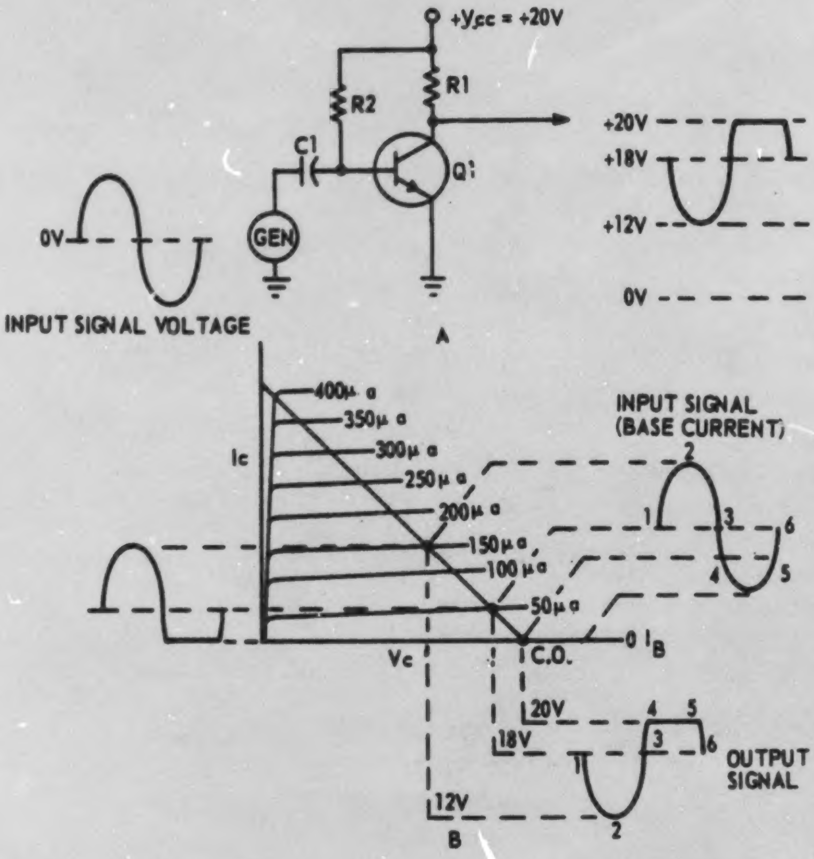
Figure 7-17. Double Zener Diode Limiter


+Vcc = +20V
R1
R2
C1
Q1
GEN
0V
INPUT SIGNAL VOLTAGE
A
+20V
+18V
+12V
0V
Ic
400μ a
350μ a
300μ a
250μ a
200μ a
150μ a
100μ a
50μ a
0 IB
Vc
C.O.
INPUT SIGNAL
(BASE CURRENT)
1
2
3
4
5
6
20V
18V
12V
OUTPUT
SIGNAL
B

REP4-1458

Figure 7-18. NPN Cutoff Limiting Circuit and Waveforms

7-42. Figure 7-17 shows another arrangement of zener limiting. Two zener diodes are connected "back-to-back." Each is an 8-volt zener diode. When the positive alternation of the input signal is applied (T0 to T1), CR1 is forward biased and acts like a short. At the same time, CR2 is reverse biased and acts as a large resistance. The output follows the input.

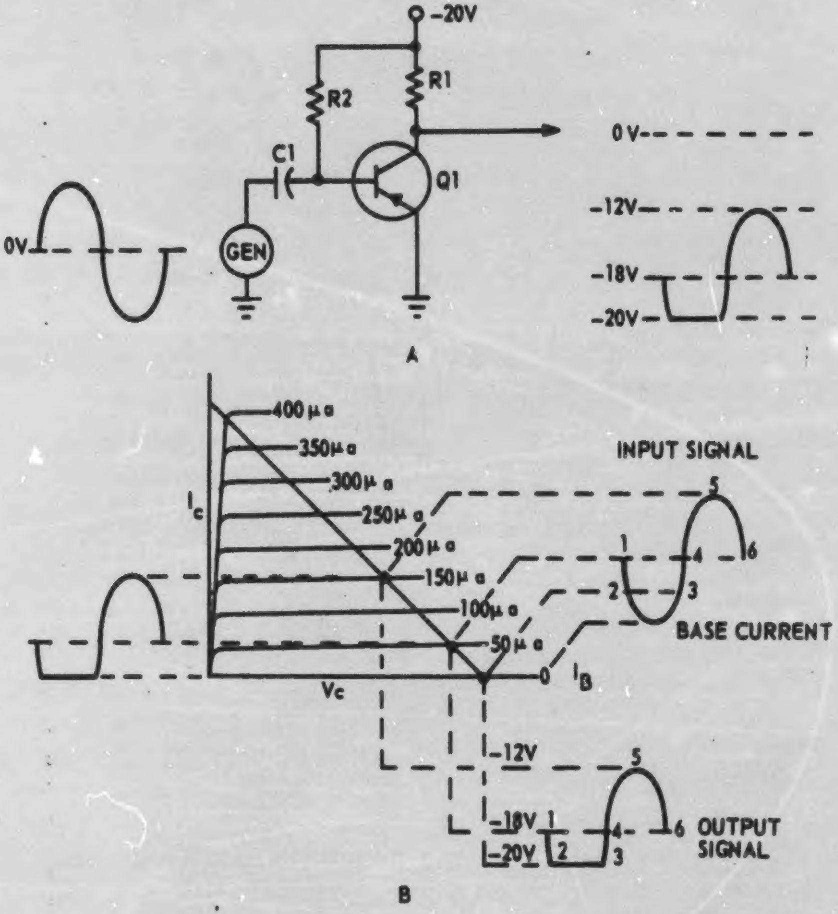
7-43. At T1, CR2 reaches its regulating area and conducts; this limits the output from going any more positive. From T1 to T2, the output is +8 volts. From T2 to T3, the output again follows the input.

7-44. At T3, CR2 becomes forward biased and acts like a short, but CR1 is reverse biased. Between T3 and T4, therefore, the output follows the input. At T4, CR2 reaches its regulating point and conducts; this limits the output from going more negative. From T4 to T5, the output is -8 volts. From T5 to T6, the output again follows the input.

7-45. Another method of limiting signals is operating transistors at cutoff or at saturation. This may be accomplished with either NPN or PNP transistors.

7-46. NPN Transistor Cutoff Limiting

7-47. Figure 7-18A shows an NPN transistor cutoff limiter. Notice that V_{CC} is positive.


-20V
R2
R1
C1
Q1
GEN
0V
0 V
-12V
-18V
-20V
A
400µa
350µa
300µa
250µa
200µa
150µa
100µa
50µa
0
I_c
V_c
I_B
INPUT SIGNAL
BASE CURRENT
1
2
3
4
5
6
-12V
-18V
-20V
OUTPUT SIGNAL
B

REP4-1459

Figure 7-19. PNP Cutoff Limiting Circuit and Waveforms

Assume the value of forward bias is 50 microamps which places the operating point at the lower portion of the load line. (Figure 7-18B.)

7-48. Let's now consider each half-cycle of the input to determine how the output is produced. At point 1 of the input signal the transistor is conducting, and collector voltage is 18 volts. From point 1 to point 2, the input aids, and base current increases to 150 microamps. During this time, collector voltage swings in the negative direction decreasing to 12 volts.

7-49. From point 2 to point 3, the input allows the base current to return to 50 microamps and collector voltage swings back to 18 volts. Note that the positive half-cycle of the input voltage is phase inverted and amplified, and becomes the negative half-cycle of the output signal. There is no limiting.

7-50. Between point 3 and point 4, the negative input voltage opposes base current and at point 4 drives the transistor into cutoff. During this time collector voltage swings in the positive direction, increasing to 20 volts. From point 4 to point 5, the input signal holds the transistor below cutoff and collector voltage remains at the V_{CC} level (+20 volts), and limiting takes place. If the forward bias was decreased, more of the input signal would hold the transistor below cutoff, and the amount of limiting would increase.

7-51. From point 5 to point 6, the input signal allows base current to return to 50 microamps and collector voltage swings back to 18 volts. Note that cutoff limiting in an NPN transistor circuit limits the top of the collector voltage waveshape during the time the transistor is cut off.

7-52. PNP Transistor Cutoff Limiting

7-53. Let's compare the PNP curoff limiter in Figure 7-19B to the NPN cutoff limiter in Figure 7-18. Notice that the collector supply voltage has been reversed and the bottom of the output waveshape is now limited. Again, only a small forward bias is applied (50 microamps).

7-54. Let's consider each half-cycle of the input to determine how the output is produced. At point 1 of the input signal, the transistor is conducting and V_c is -18 volts. From point 1 to point 2, the input voltage opposes base current and drives the transistor into cutoff at point 2. During this time collector voltage swings in the negative direction, going to -20 volts. From point 2 to point 3, the input signal holds the transistor below cutoff, and collector voltage remains at the V_{CC} level (-20 volts). Limiting is now taking place. If forward bias decreases, limiting will increase.

7-55. From point 3 to point 4, the input signal allows base current to return to 50 microamps and collector voltage swings back to -18 volts. Note that cutoff limiting in a PNP transistor circuit limits the bottom of the collector voltage waveshape during the time the transistor is cut off.

7-56. From point 4 to point 5, the input aids base current and base current increases to 150 microamps. During this time the collector voltage swings in the positive direction (less negative) to -12 volts.

7-57. From point 5 to point 6, the input signal allows the base current to return to 50 microamps and collector voltage swings back to -18 volts. No limiting occurs.

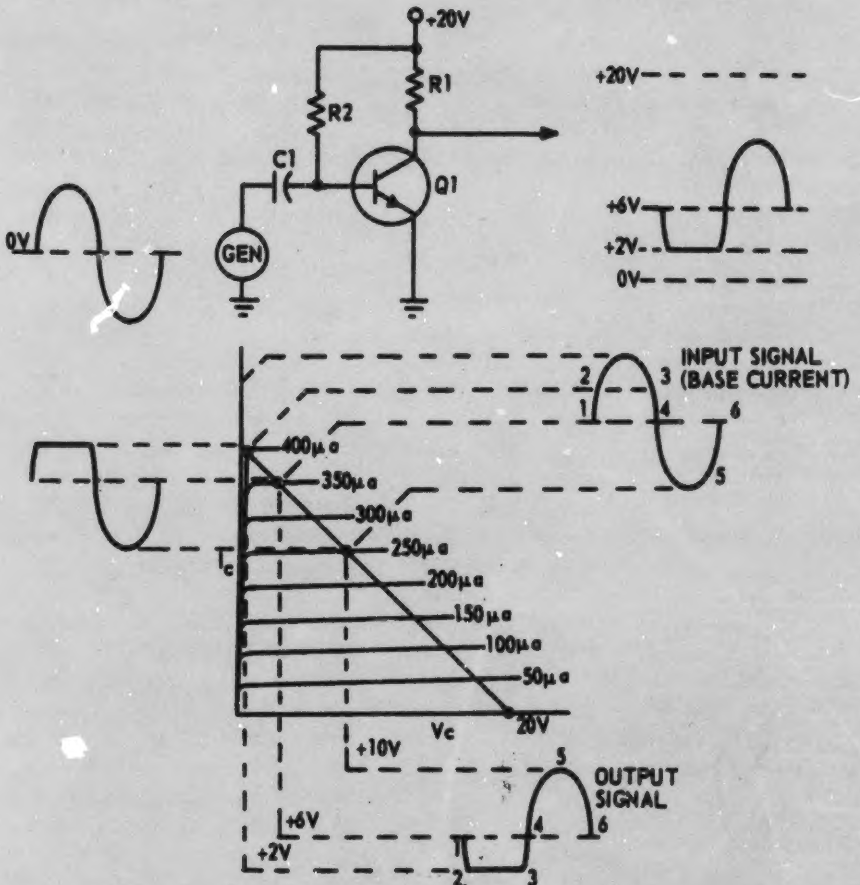
7-58. NPN Transistor Saturation Limiting

7-59. Look at the schematic diagram for an NPN saturation limiter in Figure 7-20. The amount of forward bias needed in a saturation limiter is greater than the forward bias needed in a cutoff limiter. The load line shows the operating point close to the saturation area. Locate where the 350 microamp base current line crosses the load line. This operating point will allow the input signal to drive the NPN transistor into saturation.

7-60. Let's now consider each half-cycle of the input to determine the output. At point 1 of the input signal, the transistor is conducting and collector voltage is 6 volts. From point 1 to point 2, the input aids base current and drives the transistor to saturation. During this time collector voltage swings in the negative direction, decreasing to a minimum value of +2 volts. From point 2 to point 3, the input signal holds the transistor beyond saturation and collector voltage remains at a steady voltage of +2 volts. From point 2 to point 3, the input signal holds the transistor beyond saturation and collector voltage remains at a steady voltage of +2 volts. Limiting is taking place. If forward bias was increased, more of the input would hold the transistor beyond saturation and the amount of limiting would increase.

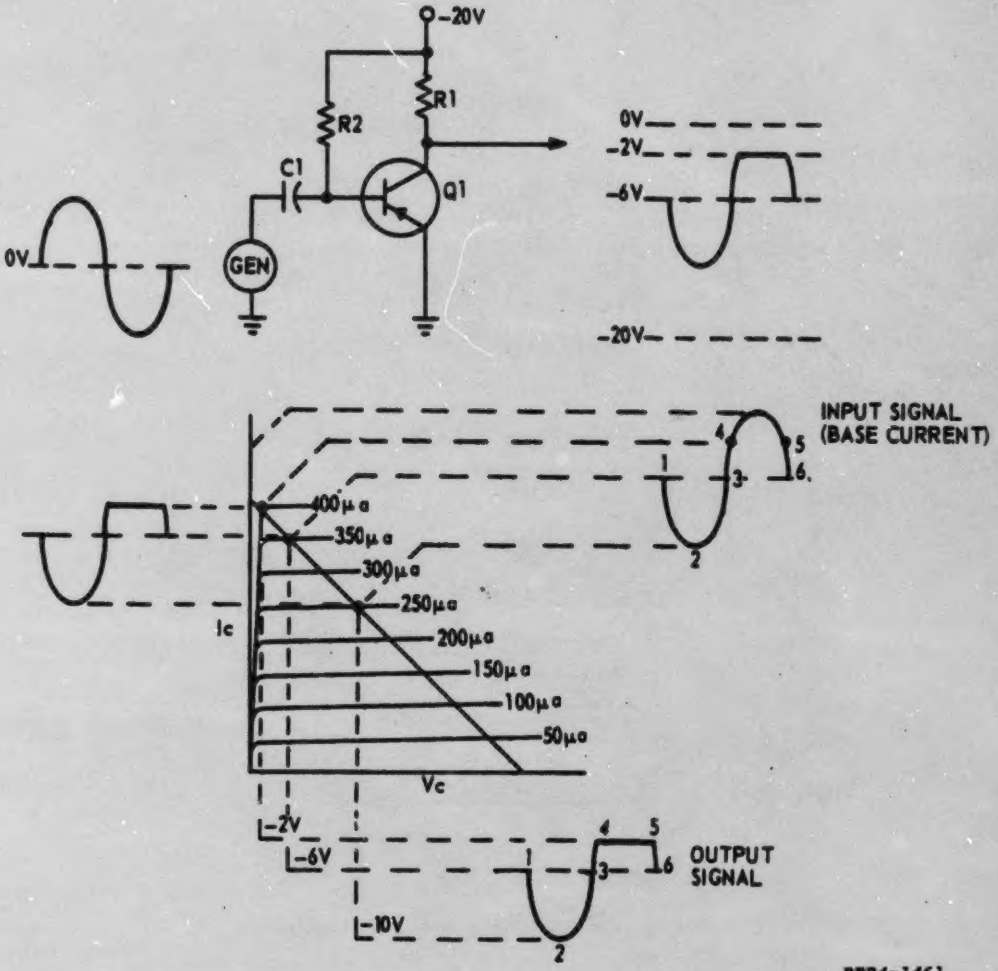
7-61. From point 3 to point 4, the input signal allows base current to return to 350 microamps and collector voltage swings back to 6 volts. Note that saturation limiting in an NPN transistor circuit limits the bottom of the collector voltage waveshape.

7-62. From point 4 to point 5, the input causes base current to decrease to 250 microamps. During this time collector voltage swings in the positive direction, increasing


+20V
R1
R2
C1
Q1
GEN
0V
+20V
+6V
+2V
0V
INPUT SIGNAL
(BASE CURRENT)
1
2
3
4
5
6
400μa
350μa
300μa
250μa
200μa
150μa
100μa
50μa
Ic
Vc
20V
+10V
+6V
+2V
OUTPUT
SIGNAL
1
2
3
4
5
6

REP4-1460

Figure 7-20. NPN Saturation Limiter Circuit and Waveforms


-20V
R1
R2
C1
Q1
GEN
0V
0V
-2V
-6V
-20V
INPUT SIGNAL
(BASE CURRENT)
1
2
3
4
5
6
400μa
350μa
300μa
250μa
200μa
150μa
100μa
50μa
Ic
Vc
-2V
-6V
-10V
OUTPUT
SIGNAL
1
2
3
4
5
6

REP4-1461

Figure 7-21. PNP Saturation Limiter Circuit and Waveforms

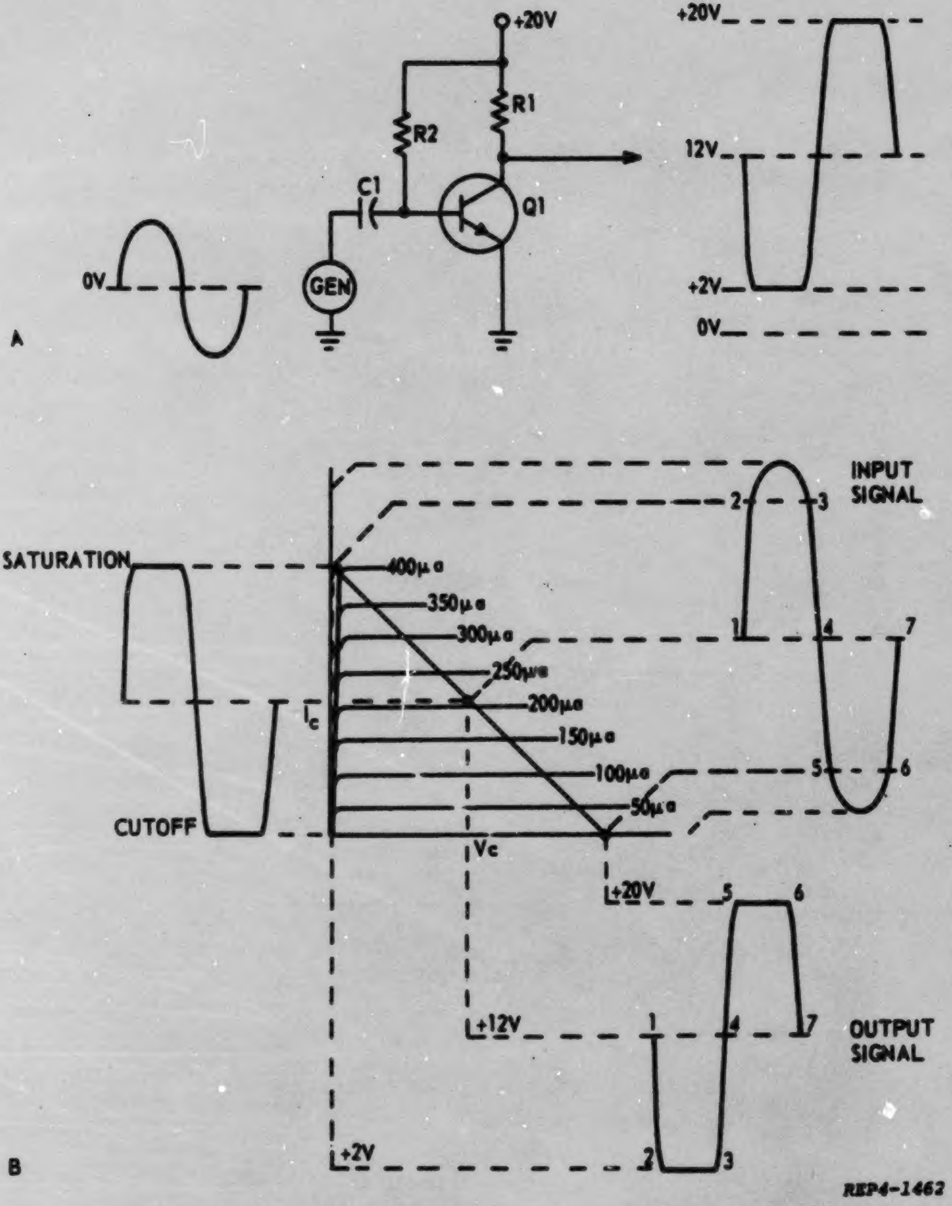

+20V
R1
R2
C1
Q1
GEN
0V
A
+20V
12V
+2V
0V
INPUT SIGNAL
SATURATION
400μa
350μa
300μa
250μa
200μa
150μa
100μa
50μa
I_c
CUTOFF
V_c
+20V
+12V
+2V
OUTPUT SIGNAL
1
2
3
4
5
6
7
B
REP4-1462

Figure 7-22. NPN Overdriven Limiter Circuit and Waveforms

to +10 volts. From point 5 to point 6, the input allows the base current to return to 350 microamps, and collector voltage swings back to 6 volts.

7-63. PNP Transistor Saturation Limiting

7-64. Let's now look at the PNP saturation limiter in Figure 7-21. Notice that the output waveshape is phase inverted, as in the NPN circuit, but saturation limiting clips the top of the waveshape instead of the bottom.

7-65. Now, look at the load line for saturation limiting shown in Figure 7-21. Locate where the 350 microamp base current curve crosses the load line. This operating point will allow the input to drive the PNP transistor into saturation. Note: An increase in input (base) voltage causes a decrease in input signal (base) current.

7-66. Consider each half-cycle of the input to determine how the output is produced. At point 1 of the input signal, the transistor is conducting and collector voltage is -6 volts. Follow the input and output signals from point 1 to points 2, 3, and 4. There is no limiting during this tme.

7-67. At point 4, the input drives the transistor to saturation; collector voltage swings in the positive direction, decreasing to a minimum value of -2 volts. From point 4 to point 5, the input signal holds the transistor beyond saturation, and collector voltage remains at a steady value of -2 volts. Note that saturation limiting in a PNP transistor circuit limits the top of the collector voltage waveshape. Also, note that an increase in the forward bias would increase the amount of signal that held the transistor beyond the saturation region on the load line and would increase limiting.

7-68. From point 5 to point 6, the input signal allows base current to return to 350 microamps and collector voltage swings back to -6 volts.

7-69. NPN Transistor Overdriven Limiting

7-70. Figure 7-22 shows an overdriven limiter. Input signal amplitude is sufficient to drive the transistor into both cutoff and saturation. The operating point is where the load line crosses the 200 microamp base current curve. A strong signal input drives the NPN transistor above and below this point, into both cutoff and saturation.

7-71. At point 1 of the input signal the transistor is conducting and collector voltage is 12 volts. At point 2, the input drives the transistor to saturation. During this time collector voltage swings in the negative direction, decreasing to a minimum value of +2 volts. From point 2 to point 3, the input signal holds the transistor beyond saturation and the collector voltage remains at a steady voltage of +2 volts.

7-72. From point 3 to point 4, the input signal allows base current to return to 200 microamps and collector voltage swings back to 12 volts. At point 5, the input drives the transistor to cutoff. During this time collector voltage swings in the positive direction, increasing to almost 20 volts. From point 5 to point 6, the input signal holds the transistor below cutoff, and the collector voltage remains at approximately the V_{CC} level (+20 volts). From point 6 to point 7, the input signal allows base current to return to 200 microamps and collector voltage swings back to 12 volts. Note that in an NPN transistor circuit, cutoff limiting occurs when the collector current is minimum and saturation limiting occurs when the collector current is maximum.

7-73. PNP Transistor Overdriven Limiting

7-74. Now use Figure 7-23 to compare the PNP overdriven limiter with the NPN overdriven limiter. Notice that the output waveshape is phase inverted in both, but PNP cutoff limiting clips the bottom of the waveshape and PNP saturation limiting clips the top of the waveshape. The load line shows the operating point the same as used with the NPN overdriven limiter, and he input signal has large amplitude.

7-75. Consider each half-cycle of the input to determine how the output is produced.

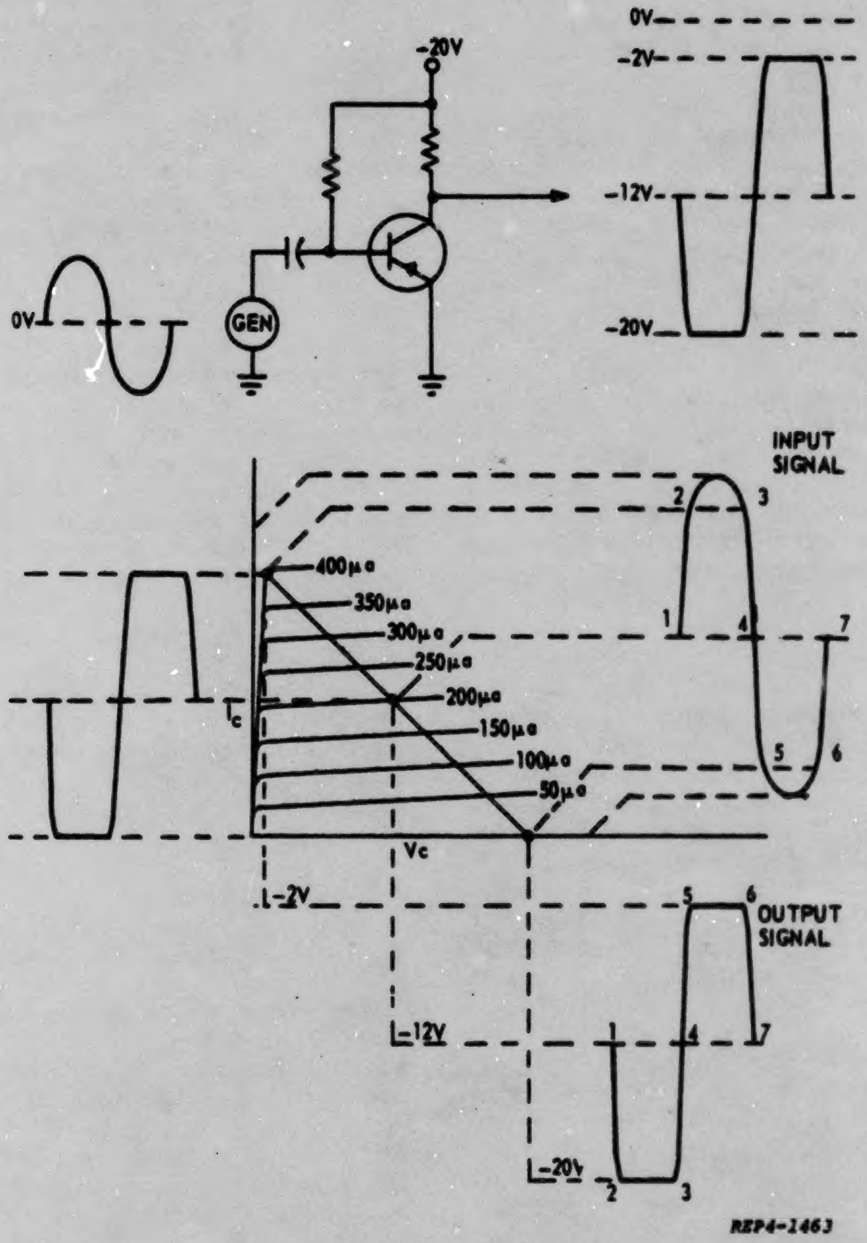

-20V
GEN
0V
0V
-2V
-12V
-20V
INPUT SIGNAL
1
2
3
4
5
6
7
400µa
350µa
300µa
250µa
200µa
150µa
100µa
50µa
Ic
Vc
-2V
-12V
-20V
OUTPUT SIGNAL
1
2
3
4
5
6
7
REP4-1463

Figure 7-23. PNP Overdriven Limiter Circuit and Waveforms

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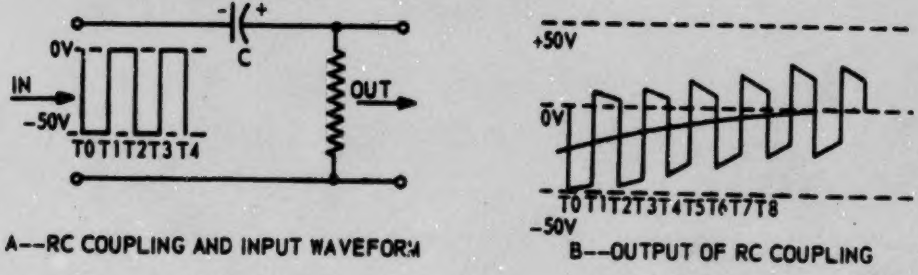


A--RC COUPLING AND INPUT WAVEFORM

B--OUTPUT OF RC COUPLING

REP4-1464

Figure 7-24. RC Coupling

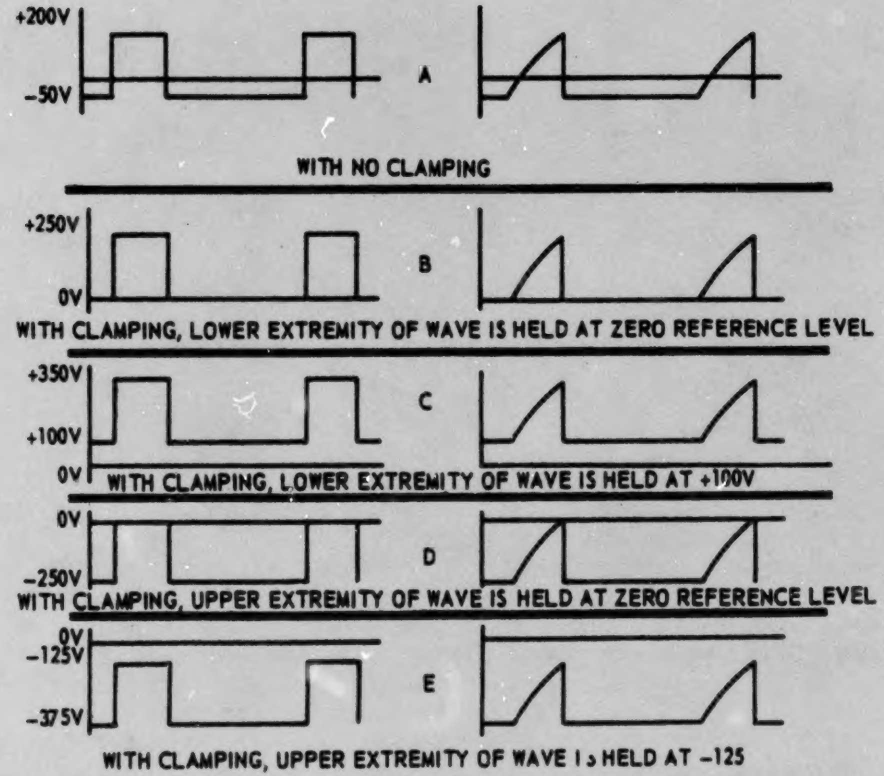
At point 1 of the input signal, the transistor is conducting and collector voltage is -12 volts. At point 2, the input voltage drives the transistor to cutoff. During this time, collector voltage swings in the negative direction to almost -20 volts. From point 2 to point 3, the input signal holds the transistor below cutoff and collector voltage remains at approximately the V_{CC} level (-20 volts).

7-76. From point 3 to point 4, the input signal allows the base current to return to 200 microamps and collector voltage swings back to -12 volts. At point 5, the input voltage drives the transistor to saturation. During this time collector voltage swings in the positive direction, decreasing to a minimum value of -2 volts. From point 5 to point 6, the input signal holds the transistor beyond saturation, and the collector voltage remains at a steady voltage of -2 volts. From point 6 to point 7, the input allows base current to return to 200 microamps and collector voltage swings back to -12 volts.

7-77. Clampers

7-78. Before we discuss clampers, it is necessary that we review series RC circuits. Series RC circuits are widely used for coupling or transferring signals from one stage to another. If the time constant of the coupling circuit is long enough, the shape of the input and output voltage waveforms will be almost identical. However, the output wave's DC reference level may be different.

7-79. Figure 7-24 shows a typical RC coupling circuit in which the output reference level has been changed to zero. In this circuit the values of R and C are such that the capacitor will charge to 20 percent of the applied voltage during the time from the leading to lagging edge of the waveshape (T0 to T1). With this in mind, let's consider the operation of the circuit. At time T0, the input voltage is -50 volts and the capacitor starts charging. At the first instant the voltage across C is zero and the voltage across R is 50 volts negative with respect to ground. Now, as C charges, the voltage across C increases and the voltage across R, which is the output voltage, begins to drop at the same rate. At time T1, the capacitor has charged to 20 percent of the -50 volts input, or 10 volts. Now, the input voltage goes to zero volts, and the capacitor must discharge. It discharges through the low impedance of the signal source, and through R, developing a 10-volt output across R at the first instant. From T1 to T2, C discharges 20 percent of the original 10-volt charge. Thus, C discharges to 8 volts and the output voltage also drops to 8 volts. At T2 the input signal goes to -50 volts again. This 50 volts is in series opposition

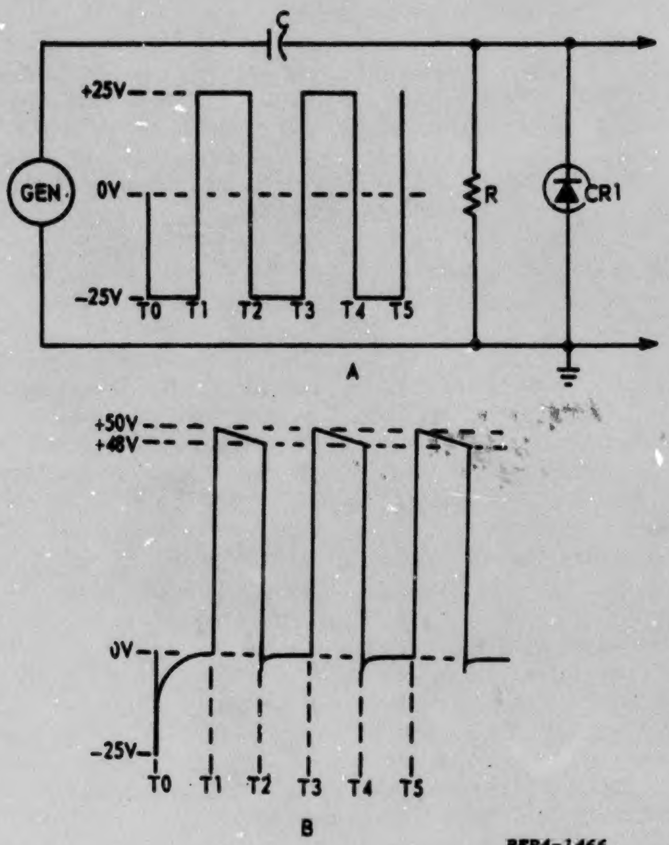

+200V
-50V
A
WITH NO CLAMPING
+250V
0V
B
WITH CLAMPING, LOWER EXTREMITY OF WAVE IS HELD AT ZERO REFERENCE LEVEL
+350V
+100V
0V
C
WITH CLAMPING, LOWER EXTREMITY OF WAVE IS HELD AT +100V
0V
-250V
D
WITH CLAMPING, UPPER EXTREMITY OF WAVE IS HELD AT ZERO REFERENCE LEVEL
0V
-125V
-375V
E
WITH CLAMPING, UPPER EXTREMITY OF WAVE IS HELD AT -125

REP4-1465

Figure 7-25. Clamping Waveforms

to the 8-volts charge on the capacitor. Thus, the voltage across *R* is 42 volts. Notice that this value of voltage is smaller in amplitude than the amplitude of the output voltage which occurred at T0. Capacitor C charges from 8 to 16 volts. If we were to continue to follow the operation of the circuit, we would find that the output waveshape would become exactly distributed around the zero reference point. At this tme, the circuit operation reaches a stable point. Note that our output waveshape has the same amplitude and approximately the same shape as the input waveshape, but now "rides" equally above and below zero.

7-80. There are certain applications in electronics which require that the upper or lower extremity of a wave be fixed at a specified value. A clamping circuit is one which effectively clamps or ties down the upper or lower extremity of a wave to a fixed DC potential. This circuit is also known as a "direct current restorer" or a "base-line stabilizer." Figure 7-25 illustrates the result of clamping an input signal to various clamping levels. These clamped waveshapes are idealized, but they do illustrate an important point about clamping: Clamping does not change the amplitude or shape of the input wave.



REP4-1466

Figure 7-26. Positive Clamper Circuit and Waveforms

7-81. Positive Clamper

7-82. Figure 7-26A illustrates the circuit of a positive diode clamper. Resistor R provides a discharge path for C. This resistance is large in value so the discharge time of C will be very long. The diode provides a very fast charge path for C. Capacitor C, once it becomes charged, will act as a source of voltage. The input waveshape shown in Figure 7-25A is a square wave which varies between +25 volts and -25 volts.

7-83. In order to fully understand the operation of this circuit, we will consider each portion of the input waveshape and determine its corresponding output waveshape. The waveshapes are shown in Figure 7-26B. Basically, we use Kirchhoff's Law: The algebraic sum of the voltage drops around a closed loop is zero at any instant.

7-84. At time T0, the -25 volt input signal applied to the circuit appears across R (the capacitor is a short at the first instant) and CR1. The -25 volts felt felt across CR1 makes the cathode negative with respect to the anode, and the diode conducts heavily.

7-85. C charges quickly through the small resistance of CR1. As the voltage across C increases, the output voltage decreases at the same rate. The voltage across C reaches 25 volts and the output voltage becomes zero.

7-86. At time T1, the 25 volts across the capacitor and the +25 volts from the input signal are series aiding. Thus, +50 volts appears across R and CR1 in parallel. At this time the cathode of CR1 is positive with respect to the anode, and the diode does not conduct. During time T1 to T2, C discharges to approximately 23 volts (due to the size of R and C) and the output voltage drops from +50 volts to +48 volts.

7-87. At time T2 the input signal changes to -25V, series opposing the 23 volts across C. This leaves an output voltage of -2 volts. The cathode of CR1 is negative with respect to the anode and CR1 conducts. During time T2 to T3, C charges quickly through CR1, from 23 volts to 25 volts, and the output voltage changes from -2 volts to 0 volts.

7-88. At time T3, the input signal and E_C are again series aiding. Thus, the output voltage felt across R and CR1 is again +50 volts. During time T3 to T4, C discharges 2 volts through R. Notice how the circuit operation from T3 to T4 is the same as it was from T1 to T2. The circuit operation in each square-wave cycle repeats the operation which occurred from T2 to T4.

7-89. By comparing the input waveshape, Figure 7-26A, with the output waveshape, Figure 7-26B, note the following important facts: (1) the peak-to-peak amplitude of the input waveshape has not been changed by the clamper circuit, (2) the shape of the input waveshape has not been changed, for all practical purposes, by the action of the clamper circuit, and (3) the output waveshape is now above zero whereas the input waveshape reference level is zero. Thus, the lower extremity of the input waveshape reference level is zero. Thus, the lower extremity of the input waveshape has been clamped to a DC potential of zero volts.

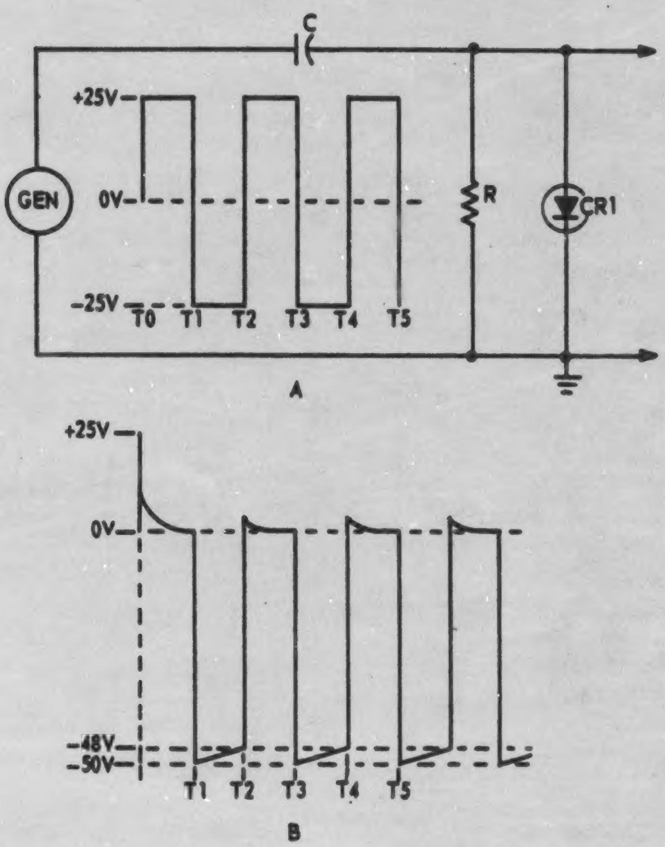
7-90. A summary of the circuit operation is as follows: The capacitor initially charges to 25 volts through the small resistance of the diode. Once the capacitor is charged, it does not have time to discharge any appreciable amount before the next charge cycle. Thus, the 25-volt charge across the capacitor adds algebraically to the input signal to produce an output signal which varies between 0 and +50 volts. It is a "positive clamper" since the output waveshape is above zero and the bottom of the output waveshape is clamped at zero.

7-91. The circuit described is "self-adjusting" in that the bottom of the output waveform remains clamped at zero during changes in input signal amplitude, and the output waveshape retains the form and peak-to-peak amplitude of the input waveshape. When the input amplitude becomes greater, the capacitor's charge becomes greater and the output has a larger amplitude. When the input amplitude decreases, the capacitor does not charge so high, clamping a lower voltage output. The capacitor charge changes with signal strength.

7-92. The size of R and C have a direct effect upon the clamper's operation. Because of the small resistance of the diode, the capacitor charge time is short. If either R or C is made smaller, the capacitor discharges faster.

7-93. For the capacitor to quickly discharge to a lower voltage is an ADVANTAGE when the amplitude of the input waveshape is suddenly reduced. For normal clamper operation, however, quick discharge time is a DISADVANTAGE because one objective of clamping is to keep the output waveshape like the input waveshape. If the small capacitor allows a relatively large amount of the voltage across it to discharge with each cycle, distortion occurs in the output waveshape, and a larger portion of the waveshape appears on the wrong side of the reference line.

7-94. Increasing the resistor size increases the discharge time. This causes the capacitor to discharge more slowly, producing an output waveshape which is a better reproduction of the input waveshape. A disadvantage is that the large resistor increases the discharge time of the capacitor and slows the self-adjustment rate of the circuit in case a sudden DROP in input amplitude should occur. The large resistor has no effect on self-



REP4-1468

Figure 7-27. Negative Clamper Circuit and Waveforms

adjustment with a sudden *RISE* in input amplitude, because the capacitor charges through the small resistance of the conducting diode.

7-95. Circuits often incorporate a compromise between a short *RC* time constant for self-adjustment and a long *RC* time constant for less distortion. A point to observe is that the reverse resistance of the diode sometimes replaces the physical resistor in the discharge path of the capacitor.

7-96. Negative Clamper

7-97. Figure 7-27A illustrates the circuit of a negative diode clamper. Compare this with Figure 7-26. The diode is reversed with reference to ground. Like the positive clamper, resistor *R* provides a discharge path for C, and the resistance must be a value to make the discharge time of C very long. The diode provides a fast charge path for C. Once C becomes charged, it acts as a source of voltage which will help determine the maximum and minimum voltage levels of the output waveshape. The input waveshape shown in Figure 7-27A is a square wave which varies between +25 and -25 volts.

7-98. Again, we will consider each portion of the input waveshape and determine its corresponding output waveshape. The waveshapes are shown in Figure 7-27B. You will

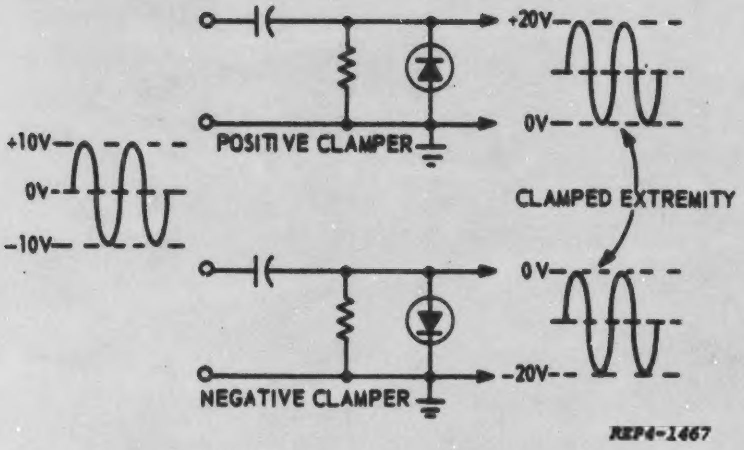


Figure 7-28. Clamper Circuit Waveforms

find that the operation of the negative clamper is like that of the positive clamper except for the reversal of polarities.

7-99. At time T0, the +25 volts input signal applied to the circuit appears across R1 and CR1. The 25 volts felt across CR1 makes the anode positive with respect to the cathode and CR1 conducts heavily. Diode resistance is very small so C charges quickly. As the voltage across C increases, the output voltage decreases. The voltage across C reaches 25 volts quickly and during most of time T0 to T1 the output voltage is zero.

7-100. At time T1, the voltage across the capacitor and the input voltage are series aiding. Thus, -50 volts appears as the output voltage.

7-101. At this time, the diode is reverse biased and does not conduct. Due to the size of R and C, the capacitor discharges down to approximately 23 volts during time T1 to T2. Using Kirchhoff's voltage law, the output voltage decreases from -50 volts to -48 volts.

7-102. At time T2 the input signal, +25 volts, and the 23 volts across C are series opposing. Thus, the output voltage is +2 volts.

7-103. The anode of CR1 is positive with respect to the cathode and CR1 will conduct. During time T2 to T3, C charges quickly from 23 to 25 volts through CR1. At the same time the output voltage falls from +2 volts to 0 volts.

7-104. At time T3, the input and E_C are series aiding. Thus, the output voltage is -50 volts. During time T3 to T4, CR1 is reverse biased and C discharges through R. Notice how the circuit operation is the same as it was from T1 until T2. The circuit operation for each next square wave cycle duplicates the operation which occurred from T1 to t3.

7-105. As was the case with the positive clamper, the amplitude and shape of the output waveshape is almost identical to that of the input waveshape. Note here, however, that the upper extremity of the ouput waveshape is clamped to zero. That is, the output waveshape, for all practical purposes, lies entirely below the zero reference level.

7-106. We have used only the square wave input signal to simplify the explanation of the clamping circuits. Clamping circuit input waveshapes may be of any shape and may be distributed in any manner with respect to any referencelevel. Ideally, the output waveshape is an exact duplication of the input in shape and amplitude, clamped above (positive) or below (negative) the reference level.

7-107. Figure 7-28 illustrates a sine wave input applied to positive and negative clampers. The important points to note here are that: (1) the outputs have the same shape and peak-to-peak amplitude as the input waveshapes, (2) the lower extremity of the positive clamper output touches the zero reference level and the rest of the waveshape is above the reference level, and (3) the upper extremity of the negative clamper output touches the zero reference level and the rest of the waveshape is below the zero reference level.

7-108. Follow these steps to determine clamper output waveshapes:

7-109. Determine whether the clamper is a positive or negative clamper. If the diode's cathode is connected to the capacitor, it is a positive clamper. If the diode's anode is connected to the capacitor, it is a negative clamper.

7-110. Draw the clamping reference level. With clampers studied thus far this is zero (ground).

7-111. Draw the input waveshape exactly as it is with respect to shape and peak-to-peak amplitude, but with its lower extremity on the clamping reference level for a positive clamper or its upper extremity on the clamping reference level for a negative clamper. This is now the output waveshape of the clamper circuit.

7-112. Biased Clampers

7-113. Some circuit applications require an input waveshape clamped to some DC reference level other than ground. Recall the definition of bias -- "DC voltage or current used to establish an operating point." Bias in clamper circuits sets the operating point. Biased clamping circuits operate exactly the same as the unbiased clamper circuits except for the addition of a DC bias voltage in series with the diode and resistor. The size and polarity of the bias voltage determines the output clamping reference.

7-114. Figure 7-29A illustrates the circuit of a positive clamper with positive bias.

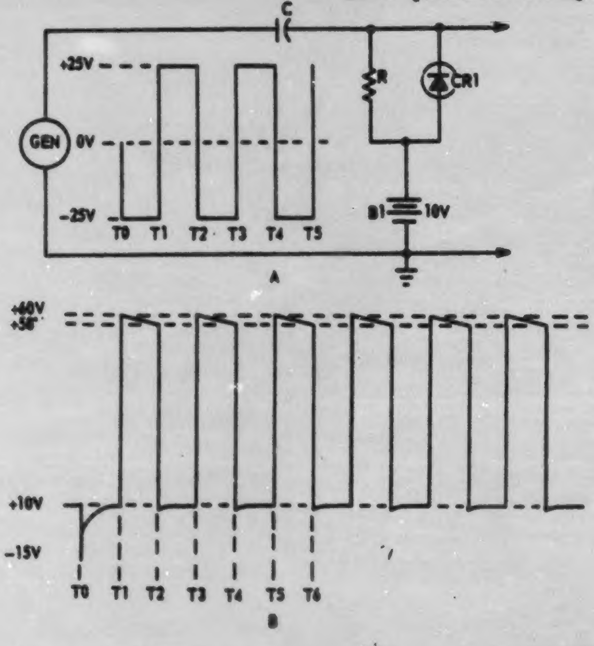


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Figure 7-29. Positive Clamper with Positive Bias

Note that this is a positive clamper because the diode's cathode is connected to the capacitor. It has positive bais since the negative side of the battery is tied to ground. The purpose and action of the capacitor, resistor, and diode are the same as in the unbiased clamper circuit.

7-115. Now, with no current through resistor *R* or the diode CR1, the voltage of the battery appears across the output terminals.

7-116. Battery B1 establishes the DC reference level at +10 volts. The input waveshape of Figure 7-29A is a square wave which varies between +25 and -25 volts. The output waveshape is shown in Figure 7-29B.

7-117. Here, as with the unbiased clampers, let's use Kirchhoff's voltage law to determine circuit operation. With no input signal, the output is +10 volts.

7-118. At time T0, the -25 volt signal applied to the circuit is instantly felt across R and CR1 in parallel. The -25 volt input signal forward biases CR1, and C will quickly charge to 35 volts, leaving +10 volts across the output terminals most of the period from T0 to T1. Mark the polarity of the charged capacitor.

7-119. At time T1- the 35 volts across the capacitor is series aiding the +25 volt input signal. Now, the output voltage is +60 volts: the voltage across *R* and CR1 is +50 volts and B1 is 10 volts. At this time, the cathode of CR1 is positive with respect to the anode and the diode will not conduct. During time T1 to T2, C will discharge slightly through the large resistance of R. Assume that, due to the size of R and C, the capacitor discharges 2 volts (from 35 volts down to 33 volts). Thus, the output voltage drops from 60 volts to +58 volts.

7-120. At time T, the -25 volt input signal and the 33 volts across C are series opposing. This makes the voltage across the output terminals +8 volts. The diode's cathode is 2 volts negative with respect to its anode so C*R*1 conducts. Again, considering the forward-biased diode as a short, C charges quickly from 33 volts to 35 volts. Most of the time from T2 to T3, therefore, we find the output voltage is +10 volts.

7-121. At time t3, the +25 volts of the input signal is series aiding the 35 volts across C, and again we find the output voltage is 60 volts.

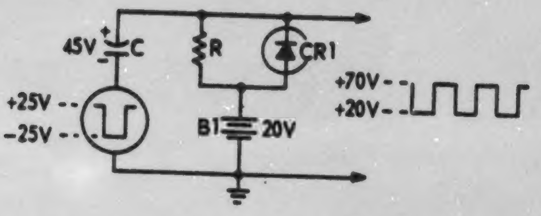
7-122. Observe that at time T3 the conditions in the circut are the same as they were at time T1. Thus, the circuit operation from T3 to T4 is the same as it was from T1 to T2. In fact, the circuit operation with every next input square-wave cycle is a duplication of the operations which occurred from T1 to T3.

7-123. By comparing the input waveshape with the output waveshape, you should note the following facts: (1) the peak-to-peak amplitude of the input waveshape has not been changed, for all practical purposes, by the action of the clamper circuit, (2) the shape of the input wave has not been changed, and (3) the output waveshape is now above +10 volts. Note that this clamping level (+10 volts) is determined by the bias battery.

7-124. A quick summary of the circuit operation is as follows: The capacitor is charged to 35 volts by the 10-volt bias battery and the -25 volt input signal which are series aiding. The capacitor does not discharge any appreciable amount before the input signal recharges the capacitor. Thus, the 35-volt charge across the capacitor adds to the input signal to produce an output signal which varies between +10 volts and +60 volts.

7-125. The self-adjusting feature and the relationship of the size of R and C are the same as with the positive unbiased clamper circuit. In fact, the only significant difference in the operation of the positively-biased positive clamper and the unbiased version of the same circuit is the battery and the clamping level.

7-126. Let's see what happens to the clamping reference level when the battery B1 is increased to 20 volts (Figure 7-30). Now the

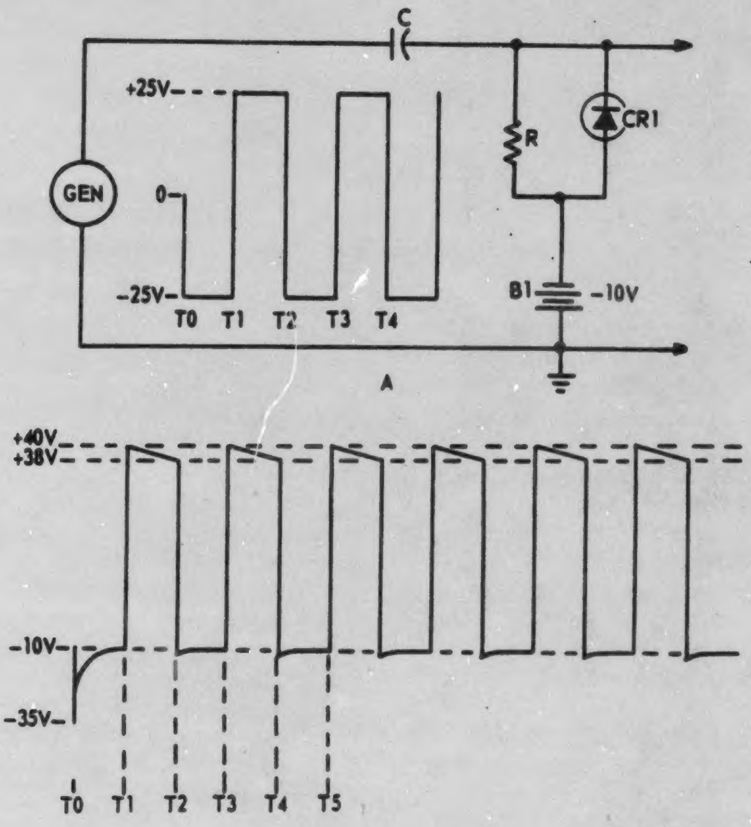


REP4-1469

Figure 7-30. Positive Clamper with Positive Bias (20V)

capacitor is initially charged to 20 volts with no input signal. The -25 volt input signal and the 20-volt battery, in series, charge the capacitor to 45 volts. The capacitor remains charged to 45 volts (for all practical purposes) since its discharge through R is almost negligible. The output voltage equals the sum of the input and capacitor voltages. When the input voltage is +25 volts, the output voltge is +70 volts. When the input voltage is -25 volts, the output is +20 volts, Thus, the output voltage varies between +20 volts and +70 volts. Note that the lower extremity of the output is clamped to +20 volts, the value of battery B1.

7-127. Figure 7-31A is the circuit of a positive clamper with negative bias. Observe that, with no input signal, the capacitor charges through *R* to the bias battery voltage and the output voltage equals that of B1. The circuit has negative bias because



REP4-1471

Figure 7-31. Positive Clamper with Negative Bias

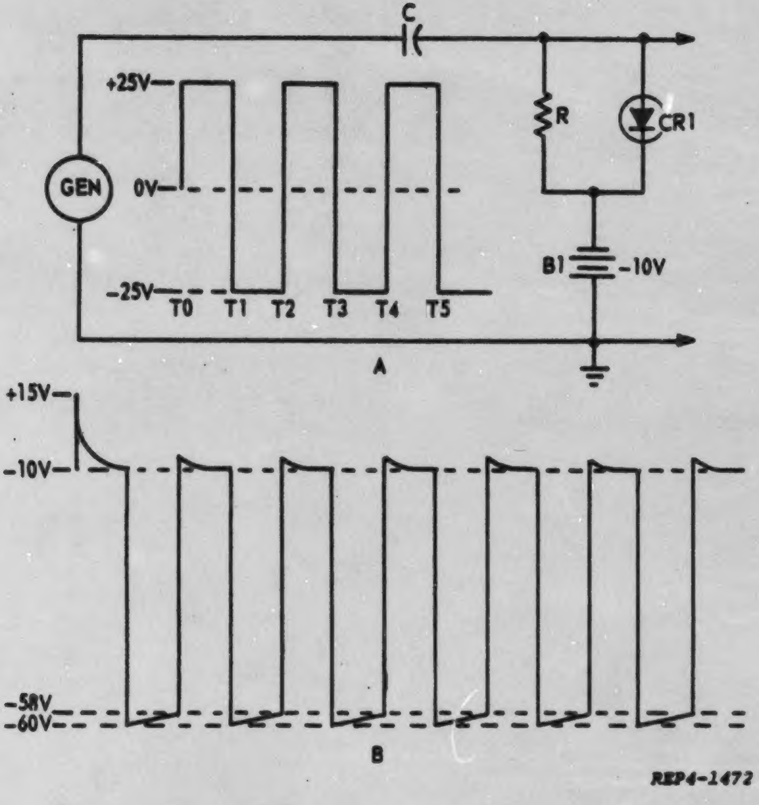
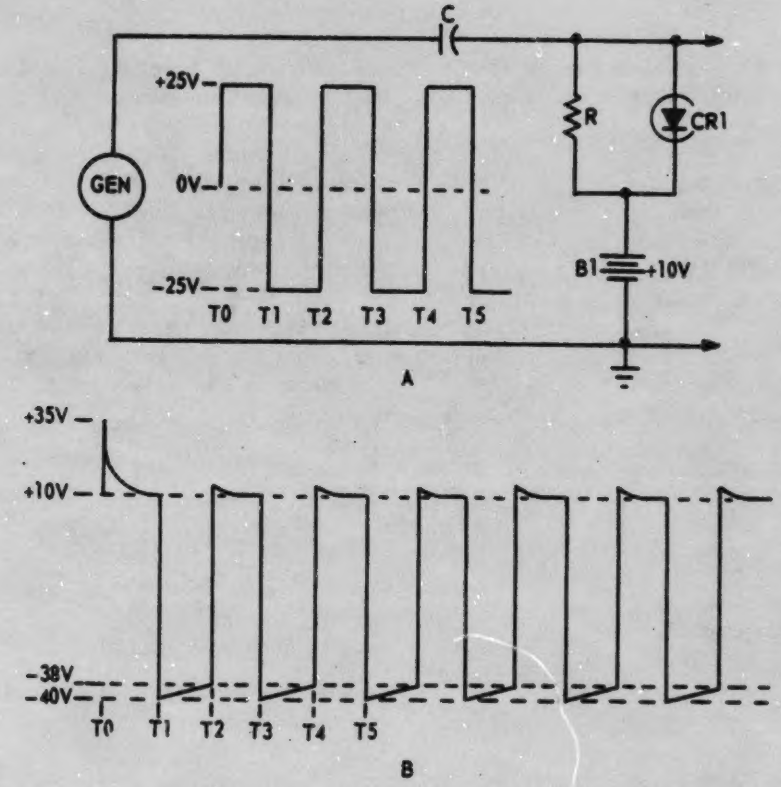


Figure 7-32. Negative Clamper with Negative Bias

the positive side of the battery is grounded. The output waveform is shown in Figure 7-31B. Study the figure carefully and note the following important points: The peak-to-peak amplitude and shape of the output wave, for all practical purposes, is the same as the input wave. The lower extremity of the output wave is now clamped to -10 volts, the value of battery B1.

7-128. A summary of the circuit operation is as follows: The capacitor is initially charged to -10 volts with no input signal, and diode CR1 does nor conduct (it conducts only when its cathode is more negative than its anode). The -25 volt input signal and the -10 volts on the battery forward bias CR1, and the capacitor charges to +15 volts. Once the capacitor is charged, it remains charged to 15 volts (for all practical purposes, since its discharge through R is negligible). The output voltage is equal to the algebraic sum of the capacitor voltage and the input voltage. The +25 volt input signal is series aiding the capacitor voltage and develops +40 volts between the output terminals. When the input voltage is -25 volts, CR1 conducts and the output voltage is -10 volts (-25 V plus +15 V). Thus, the output is clamped to -10 volts. Changing the size of the battery changes the clamping reference level to the new voltage.

7-129. Figure 7-32A is the circuit of a negative clamper with negative bias. Again with no input signal the capacitor charges to the battery voltage, and the output is negative because the positive side of the battery is grounded. Figure 7-32B shows the output of the circuit.



REP4-1473

Figure 7-33. Negative Clamper with Positive Bias

Study the figure carefully, and note the following important points: The peak-to-peak amplitude and shape of the output wave, for all practical purposes, is the same as the input wave. The output wave is now clamped to -10 volts, the value of the battery B1. Since this is a negative clamper, the upper extremity of the wave touches the -10 volt reference line (and the rest of it lies below this voltage level).

7-130. A summary of the circuit operation is as follows: The capacitor is initially charged to -10 volts with no input signal. Apply Kirchhoff's law to find that the +25-volt input signal and the 10-volt battery are in series aiding. This forward biases CR1 and the capacitor charges to -35 volts. The output voltage is equal to the sum of the capacitor voltage and the input voltage. Thus, the output voltage varies between -10 volts and -60 volts, and the waveshape is clamped to -10 volts.

7-131. Figure 7-33A illustrates the circuit of a negative clamper with positive bias. With no input signal the capacitor charges to the battery voltage, and the output is positive because the negative side of the battery is grounded. Figure 7-33B illustrates the output of the circuit. Study the figure carefully, and note the following important points: The peak-to-peak amplitude and shape of the output wave, for all practical purposes, are the same as the input wave. The output wave is now clamped to +10 volts, the value of battery B1. Being a negative clamper (emitter to ground), the top of the output wave touches the +10-volt reference line.

7-132. A summary of the circuit operation is as follows: With no input signal the capacitor charges to 10 volts. The +25 volt input signal forward biases CR1 and, with the 10-volt battery in series, charges the capacitor to 15 volts. Once charged the capacitor remains charged, for all practical purposes, since its discharge through R is almost negligible. The output voltage is equal to the algebraic sum of the capacitor voltage and the input voltage. The +25-volt input signal added to -15 volt capacitor charge and the -25 volt input signal added to the -15 volt charge cause the output voltage to vary between +10 volts and -40 volts. The waveshape is negatively clamped to +10 volts. The battery voltage sets the clamping reference level. Positive clamping sets the waveshape above (negative peak on) the reference level, and negative clamping places the waveshape below (positive peak on) the reference level.

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Technical Training

Electronic Principles (Modular Self-Paced)

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DIGESTS

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CONTENTS

MODULE	TITLE	PAGE
42	Principles of Oscillation	1
43	Solid State LC Oscillators	2
44	Solid State RC Oscillators	3
45	Solid State Frequency Multipliers	5
46	Solid State Pulsed and Blocking Oscillators	6
47	Solid State Multivibrators	9
49	Solid State Trapezoidal Generators	16
50	Solid State Limiters and Clampers	17

Module 42

PRINCIPLES OF OSCILLATION

Electronic circuits, called oscillators, are required in practically every electronic application. Since an oscillator is nothing more than an amplifier that provides its own input signal, it is logical to study oscillators right after a study of amplifiers.

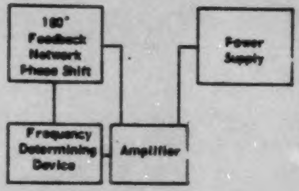
No doubt you have heard a public address system start producing an irritating squeal during use. If you have used such a system yourself, you probably know that the squeal can be eliminated either by moving the speaker or microphone or by decreasing the gain of the system amplifier. The method used to stop the public address system squeal is a reverse of one of the requirements for producing a usable sine wave signal. The PA system squeal is started by noise (a phenomenon of every electronic circuit) being generated in the amplifier. This noise is fed to the speaker and from the speaker back to the microphone. (See Chapter 2 in Student Text.) From the microphone, it is again amplified and this action continues until the noise reaches the level of a squeal.

The squeal can be stopped by moving either the microphone or speaker so that the speaker output does not feed into the microphone. The feedback path is broken. FEEDBACK, then, is one of the requirements for producing a signal. In addition, the squeal can be stopped by reducing the amplification. Therefore, AMPLIFICATION is another requirement for producing a signal. In the PA system squeal, you probably noted that the pitch of the sound varied and the frequency was changing. In other words, the PA system was producing a signal that was unwanted, and the frequency was wavering up and down. The PA system did not have the third requirement of a usable sine wave generator- A FREQUENCY-DETERMINING DEVICE.

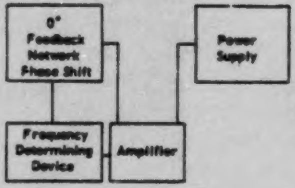
When amplification, a frequency-determining device, and feedback of the proper phase and amplitude are combined in a practical circuit, the circuit is called an oscillator. Let us discuss each of the three requirements individually.

The amplifier used as an oscillator can be any of the three different solid state configurations; common emitter, common base, or common collector. It can operate Class A, Class B, or Class C. The configuration used and class of operation depends upon system requirements, such as power, frequency, stability, and will determine the feedback arrangement.

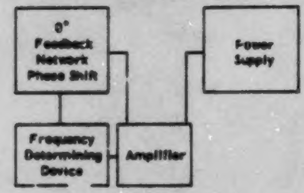
Feedback is taking a portion of the output and returning it to the input. In order to compensate for circuit losses, the feedback in an oscillator must be regenerative. You should recall that a common emitter amplifier phase shifts the signal 180° between input and output, while a common base and common collector DO NOT. Therefore, in order to have proper feedback, the signal must be phase shifted 180 degrees between collector and base when a common emitter configuration is used. No phase shift is required between output and input when either of the other two configurations are used. (see figure 42-1).


180° Feedback Network Phase Shift
Power Supply
Frequency Determining Device
Amplifier

A. Common Emitter Configuration



B. Common Collector Configuration



C. Common Base Configuration

Figure 42-1

Basically, three different methods are used for producing and maintaining a particular frequency. We have previously discussed parallel resonant LC tank circuits and their ability to "ring" or oscillate. It is very common for these circuits to be used as the frequency-determining devices in oscillators. Damping of the signal produced is offset by the amplification and regenerative feedback.

Another type of frequency-determining device (FDD) is the quartz crystal. You may recall the ability of a quartz crystal wafer to vibrate, at a frequency determined by its thickness, when voltage is applied. The crystal has the same basic qualities as the LC tank circuit. On the other hand, the Q of the crystal is much higher and frequency stability using a quartz crystal as the FDD will be much better. Resistors and capacitors are used as the FDD in lower frequency oscillators.

Review the formula

$$f_o = \frac{1}{2\pi\sqrt{LC}}$$

for frequency of an LC tank circuit. From this formula, it is quite obvious that a very low frequency oscillator would require extremely high values of inductance and capacitance, making an LC tank circuit impractical. The quartz crystal wafer would have to be thick to produce a lower frequency, and require a large potential to start it vibrating. Therefore, the ability of resistor/capacitor combinations to produce a phase shift is put to use. Since resistor/capacitor networks produce 180° phase shift at ONE frequency, they can be used to determine frequency in these ranges.

Module 43

SOLID STATE LC OSCILLATORS

Oscillators that use an LC tank circuit as the frequency determining device are termed LC oscillators. One type of LC oscillator is the series Hartley. The identifying feature of a Hartley oscillator is the tapped inductance used to obtain feedback. It is called series because the frequency determining device is in series with the DC flow. Another type is the shunt Hartley. It is identical to the series Hartley except that a load resistor has been added in the collector circuit and a capacitor has been added between the collector and LC tank circuit to block DC. (See Chapter 2 in Student Text.)

A third type of LC oscillator is the Colpitts. Its identifying feature is that regenerative feedback is obtained by tapping across a capacitive voltage divider . This arrangement provides better frequency stability by reducing the effects of changes in the transistor's interelement capacitance. (See Chapter 2 of Student Text.) The only basic change to the Colpitts oscillator to make it a Clapp oscillator refer to the figure in Student Text) is the addition of C5 in series with L1. This capacitor is added to simplify changing frequency.

The Butler crystal oscillator (see Chapter 2 of Student Text) was included in this LC oscillator section because the quartz crystal closely displays the qualities of the LC tank circuit at its resonant frequency. A quartz crystal has a much higher Q than an LC tank circuit, and the frequency stability is superior.

Take another look at the schematic diagrams referred to in the above paragraphs. It should be evident that all of these circuits have several things in common. They are as follows: (1) a method of obtaining forward bias to start and maintain transistor conduction, (2) a frequency determining device, (3) temperature stabilizing resistors in the emitter circuits, (4) bypass capacitors to prevent degeneration, (5) an output coupling method, and (6) a feedback loop to couple a portion of the output back to the input in the proper phase to sustain oscillations without damping.

Troubleshooting an oscillator is no different than troubleshooting an amplifier. We have to remember that an oscillator provides its own input signal. If the feedback

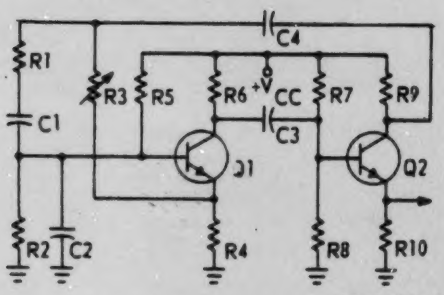


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Figure 44-2. Wien Bridge Oscillator

In the study of amplifiers you read that changing the value of the collector load resistor would change a stage's amplification factor. When the collector load resistor (R6) in figure 44-1 is changed, it varies the signal amplitude at the output by controlling the collector swing of Q1 and directly affecting the amount of feedback.

In order to begin our analysis of the Wien Bridge Oscillator, we must identify the components and paths used to couple the transistors. One path consists of the collector of Q1 through C3 to the base of Q2. The other path starts with the collector of Q2 through C4 and either by way of R3 to the emitter of Q1 or via R1/C1 to the base of Q1.

Regenerative feedback is applied to the base of Q1, and is the result of voltage variations on the base of Q1 undergoing two 180 degree phase shifts in Q1 and Q2. In other words, any signal on the base of Q1 will be developed on its collector 180 degrees out of phase. Another 180 degree phase shift will take place in Q2, and the resulting output will be fed back to the base of Q1. The feedback signal to the base of Q1 will be in phase with the original. This feedback network contains two RC circuits which are frequency sensitive. Therefore, one frequency will be regenerated and other unwanted signals in the circuit will be inhibited. R1, C1, R2, and C2 comprise the frequency determining device, and changing the value of any one or combination of these components will change the operating frequency.

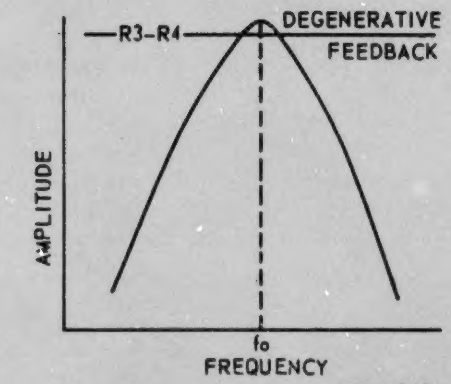

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Figure 44-3. Feedback Curve

Degenerative feedback is routed through the non-reactive (not frequency sensitive) path made up of R3, R4 and the emitter of Q1. Since this is the same signal which was used for regeneration, it will be degenerative when applied to the emitter of Q1. Figure 44-3 represents both types of feedback. The bell curve shows that regenerative feedback is maximum at the point identified f_0 and drops off above and below that frequency. The straight line labeled degenerative feedback is the same level regardless of frequency. Degenerative feedback is required to reduce the band of operating frequencies or increase stability. This is represented by the width of the bell curve at the points of intersection with the degenerative feedback line on figure 44-3. The oscillator has a variable resistor R3 in the feedback path which can control the level of degeneration and frequency stability. Refer to figure 44-3 and try to picture the change in position of the degenerative feedback line as R3 is changed. (Move up for increase and down for decrease in degeneration).

In order to produce a sine wave output, both the Phase Shift and Wien Bridge oscillators must be operated Class A. The reason for this is that neither circuit contains an LC tank circuit that will "ring" and produce a sine wave when only a small portion of a sine wave is applied to it.

For troubleshooting, refer to explanation in Volume VI of the Student Text. Laboratory Exercise 44-1 will also illustrate the effects of certain malfunctions, and demonstrate the proper methods to use in measuring output amplitude and frequency.

path is broken, the input signal is lost, and the oscillator will not function. The direct current paths should be analyzed as voltage divider networks between ground and V_{CC}, and a complete review of simple voltage divider troubleshooting might be to your advantage before attempting to troubleshoot these oscillators. If you need further troubleshooting assistance, Student Text VI Chapter 2 on troubleshooting the different oscillators offers more thorough discussion of th subject.

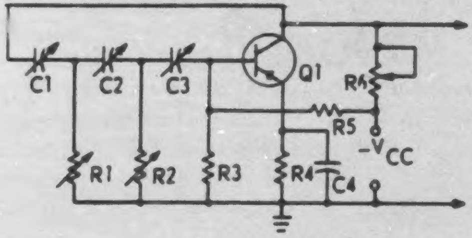
Module 44

SOLID STATE RC OSCILLATORS

During this discussion of RC oscillators, two types will be used. Figure 44-1 is called a Phase Shift oscillator, and figure 44-2 is a Wien Bridge oscillator.

Both of these circuits have distinctive identifying features. The figure 44-1 Phase Shift oscillator has three capacitors in series between the collector and base. The Wien Bridge oscillator uses two transistors, output and feedback are taken from different points and it employs regenerative and degenerative feedback.

The forward bias arrangement for both of these oscillator circuits is identical to many other oscillator and amplifier circuits you have previously studied, and no detailed explanation will be offered here. Since the frequency-determining devices for these oscillators are not similar to those previously studied, they will require an analysis. You will have to recall your study of RC time constants and the phase differences which exist across resistors and capacitors. In addition, you should keep in mind that the degree of phase shift is dependant upon frequency and the value of resistance and capacitance.



REP4-1425

Figure 44-1. Phase Shift Oscillator

Look at the Figure 44-1 schematic diagram. Note that three RC networks (C1/R1, C2/R2, C3/R3) are in the feedback path between collector and base. A common emitter configuration amplifier circuit is used and any signal appearing at the base will be shifted 180 degrees at the collector. To have regenerative feedback, the signal must be shifted another 180 degrees between the collector and base. Since the phase shift across any one RC network is always less than 90 degrees, it requires at least three RC networks to obtain a phase shift of 180 degrees. Since frequency partly determines the amount of phase shift that will occur across any RC combination, it follows that a specific combination of three RC networks will produce a shift of 180 degrees at only one frequency. Therefore, only one frequency will be shifted in phase the right amount between collector and base to be regenerative. This will be the frequency at which the oscillator will operate.

If we wish to change the oscillating frequency, we must consider altering the value of the resistance or capacitance in the RC network. If any resistor or capacitor in the feedback path is changed, the frequency that will produce a 180 degree phase shift will also change. In figure 44-1 C1, C2, C3, R1, and R2 are shown as variable, and changing one or all will cause a change in frequency. Remember that R3 is part of the frequency-determining device, but it is not variable. R3 is also part of the forward bias divider network, and should not be varied because a change in its resistance would change the forward bias and amplification factor of the transistor. It is doubtful that you will ever see a Phase Shift oscillator in use that will have all of the components variable, as shown in figure 44-1. It is depicted here so that you will realize that it is possible to change frequency by changing any of the component values in the feedback loop.

Module 45

SOLID STATE FREQUENCY MULTIPLIERS

The highest frequency at which an oscillator can function is dependent upon several limiting factors. These factors include component sizes, critical operating characteristics and restricted construction tolerances. These limitations and others are offset by using frequency multipliers. The multiplier is an electronic circuit that produces an output which is a multiple of its input frequency. The circuit can be a doubler (output frequency = input frequency X 2), a tripler (output frequency = input frequency X 3), or higher. Normally, the multiplication factor will have upper limits, but work around procedures can be used to counteract these limits.

You may recall from a previous module that square waves contain many harmonics or multiples of the fundamental frequency, and class B or C amplifiers cause squaring of the input signal. Based on these theories, it is possible to take a sine wave out of an oscillator, feed it into a class B or C amplifier and produce a distorted or squared output. This output contains large numbers of harmonics or multiples of the fundamental input frequency. The next step is to select the desired multiple and this can be accomplished by an LC tank or filter. When inserted in the amplifiers output, the filter will pass one of the frequency components contained in the square wave.

In general, the upper limit of a multiplier is the 4th harmonic due to power and stability. If the output is required to be higher than 4 times the oscillator frequency, several frequency multipliers can be cascaded together. For example, the output of an oscillator could be connected to a doubler, a tripler, and another doubler. This arrangement would give a multiplication factor of 12. (Oscillator frequency x 2 x 3 x 2 = Oscillator frequency x 12.) If the input frequency and the value of L and C of the filter is known, it is relatively simple to calculate the output frequency, and determine the multiplication factor.

For instance, with the information given on the frequency multiplier schematic figure 45-1, the output frequency and multiplication factor is calculated as follows:

First, the resonant frequency is calculated using the formula:

$$f_o = \frac{.159}{\sqrt{LC}}$$

$$= \frac{.159}{\sqrt{1 \times 10^{-3} \times 10 \times 10^{-12}}}$$

$$= \frac{.159}{\sqrt{1 \times 10^{-3} \times 1 \times 10^{-11}}}$$

$$= .159 \times 10^{7}$$

$$= 1.59 \text{ MHz}$$

The output frequency has been calculated to be 1.59 MHz or 1,590 kHz. By dividing the input frequency into the output frequency:

$$\frac{1,590 \text{ kHz}}{530 \text{ kHz}}$$

The multiplication factor is 3, and the circuit is a tripler.

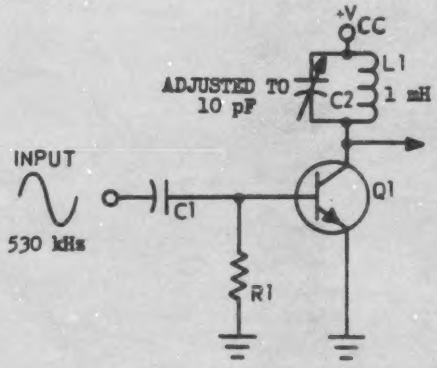


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Figure 45-1. Frequency Multiplier

Module 46

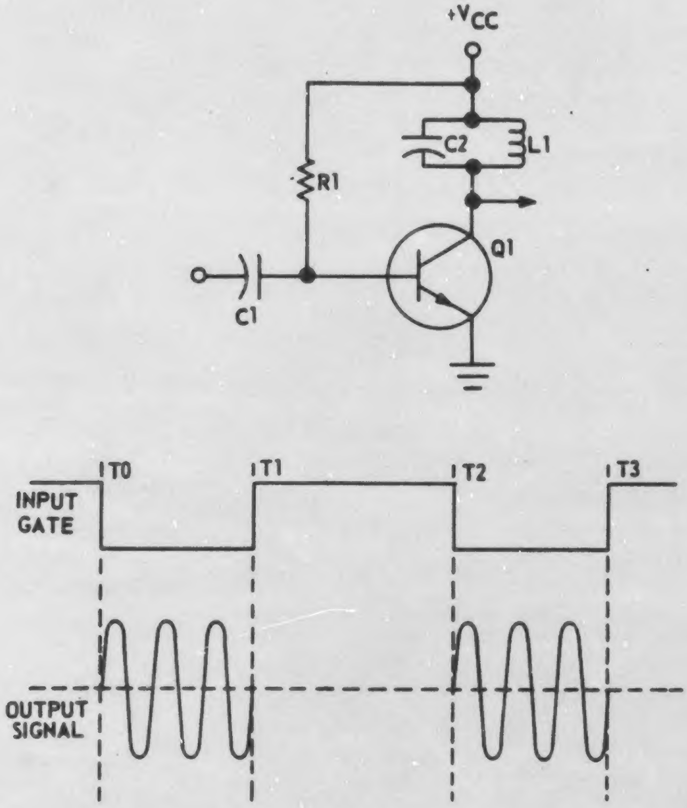
SOLID STATE PULSED AND BLOCKING OSCILLATORS

Radar transmitters require an oscillator that produces an output for a short duration, and is then turned off for a period of time. Frequency shift teletype multiplexers and telephone ringing circuits sometimes use this type circuit. Oscillators performing this function are called pulsed oscillators.

Like other types of circuits you have studied, several different varieties are available for different applications. The schematic diagram figure 46-1, with input and output signals shown, will be used during the explanation that follows.

Figure 46-1 is a schematic diagram of a collector-loaded pulsed oscillator. The circuit is a simple common emitter amplifier with C1 to provide input coupling. R1 furnishes a path for, and limits the amplitude of forward bias current, and the LC tank circuit (C2/L1) is the collector load. The name of the circuit comes from the fact that the LC tank is in the collector circuit. If placed in the emitter circuit, it would be called an emitter-loaded pulsed oscillator.

Prior to the negative gate input, Q1 is forward biased, collector current flows, and a small voltage will be dropped across L1 and C2. The negative gate is coupled through C1 to the base of Q1, overcomes the forward bias and causes it to cut off. Current stops and the tank in the collector will



REP4-795

Figure 46-1

oscillate or FLYWHEEL. The sine wave output during this period, is shown in the waveform diagram.

The frequency of the output sine wave is determined by the values of C2 and L1. The period that oscillations are produced is determined by the width of the input gate. At T1, the input gate goes in a positive direction, Q1 is again forward biased, collector current flows, and oscillations stop. At T2, the input gate again cuts Q1 off, and oscillation starts.

You should have noticed that no mention has been made of regenerative feedback. Remember that regenerative feedback was a requirement when oscillation is to be SUSTAINED over a long period. In this circuit oscillation is only required for short periods. As the width of the input gate is increased the amplitude of the sine wave will begin to decrease (dampen) and may eventually stop. If long periods of oscillation are required for a particular application, a different pulsed oscillator (with feedback) will be used. You may read about this other type by consulting paragraphs in chapter 3 of Volume VI Studen Text.

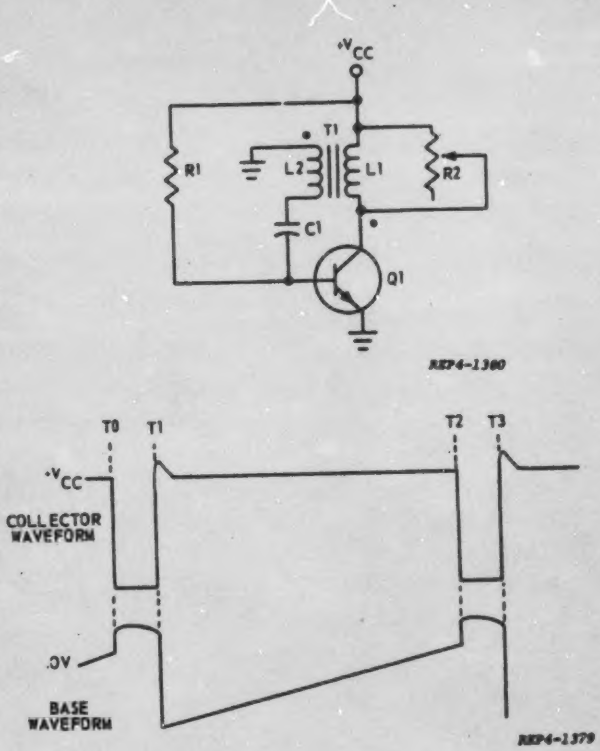


Figure 46-2. Blocking Oscillator

Blocking oscillators are used in applications which require narrow pulses with sharp leading and lagging edges. They are used as trigger generators or frequency dividers in trigger processing circuits. The name comes from the internal action of the circuit which will produce a narrow pulse and block (cutoff) itself. The simplified schematic diagram and associated waveshapes in figure 46-2 will be used to explain its operational characteristics.

Look at the circuit components and try to understand their purposes. R1 is connected between the base and V_{CC} to provide a path for forward bias and limit the amount of current. L1 and R2 form the collector load with L1 acting as the primary of a feedback transformer T-1. L2 is the secondary, and in conjunction with C1 applies feedback from the collector to the base of Q1. C1 and R1 work together to keep Q1 cutoff for a period of time (dependent upon the RC time constant) and determine the rest time (T1 to T2) of the output signal. PRT, (T0 to T2) and PRF are determined by T1, C1, and R1. Let's see how all this takes place. (Disregard R2 for the present.)

Assume that power is connected to the circuit at time T0. Forward bias is applied by R1, and collector current starts to flow. At first, L1 offers maximum opposition, drops most of the V_{CC}, and collector voltage rapidly decreases. The negative going voltage at the bottom of L1 is coupled across T1, shifted in phase and increases the conduction of Q1 by aiding the forward bias. This increase in current eventually causes transformer saturation. The time that it takes for T1 to saturate (T0 to T1) determines the pulse width. When current maximizes in L1, there is no longer a moving magnetic field, and induction into L2 stops. C1 which has charged from time T0 to T1, will now discharge through R cutting Q1 off. Q1 will remain cutoff until C1 has discharged to

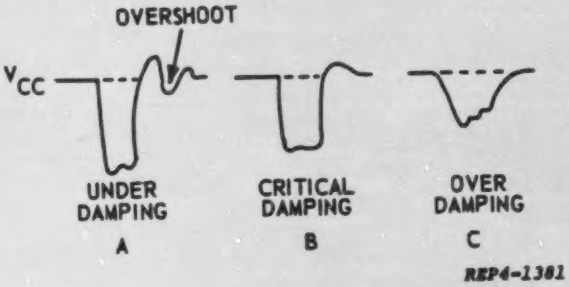
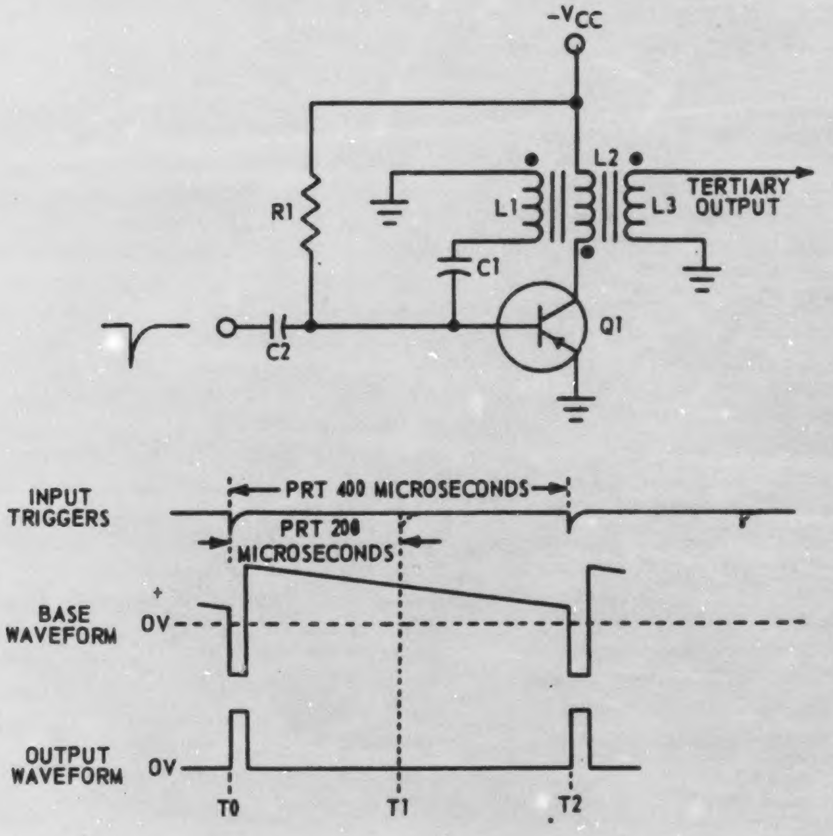

OVERSHOOT
V_{CC}
UNDER DAMPING
A
CRITICAL DAMPING
B
OVER DAMPING
C
REP4-1381

Figure 46-3. Blocking Oscillator Outputs

the forward bias level. This time is shown on the base waveform between T1 and T2. The ohmic value of R1 and the capacitance of C1 will determine the time it takes C1 to discharge, and determine the time from T1 to T2. Decreasing either C1 or R1 would decrease rest time and increasing either would increase rest time.

The collapsing magnetic field around L1 will cause ripples (ringing) on the collector waveform when the transistor is cutoff. The higher the Q of L1, the greater the amplitude of these unwanted oscillations. With R2 connected across L1, the Q of L1 can be reduced to eliminate these oscillations. The diagram of output pulses in figure 46-3 illustrates this fact. Pulse A would occur if the R2 resistance is adjusted too high. Pulse B results when R2 is properly adjusted, and pulse C is generated if R2


$-V_{CC}$
L2
TERTIARY OUTPUT
L1
L3
R1
C1
C2
Q1
INPUT TRIGGERS
PRT 400 MICROSECONDS
PRT 200 MICROSECONDS
BASE WAVEFORM
+
0V
OUTPUT WAVEFORM
0V
T0
T1
T2

REP4-1382

Figure 46-4. Triggered Blocking Oscillator

NOTES

resistance is too low. The formula for Q, considering external resistance is:

$$Q = \frac{R}{X_L}$$

The frequency of blocking oscillators is often critical. Since there are inherent inconsistencies, the circuit just discussed would be unsatisfactory for applications requiring stable frequency output. In such cases, an outside trigger can be used to control the frequency. The circuit and waveforms of figure 46-4 illustrate this stability control. The circuit operation is identical to the one just discussed, except that the trigger causes the transistor to conduct before C1 is completely discharged.

Figure 46-4 can be used to help explain the frequency dividing capability of the blocking oscillator. Input triggers combine with the base waveform to alter the natural operating frequency. At times T0 and T2, the trigger can overcome the reverse bias and cause Q1 to conduct. At T1, however, the capacitor C1 has not discharged enough to allow this to occur. The circuit responds to every second trigger, doubles the time and divides the frequency by two. For this reason the circuit may be called a 2 to 1 blocking oscillator.

Module 47

SOLID STATE MULTIVIBRATORS

In general, multivibrators produce square or rectangular waveshapes in their output. They are used in numerous applications such as timing, gating, shaping, storing, shifting, and frequency division. Because of their numerous applications, three basic types are required. However, for specialized applications, the basic types are frequently modified as required to fit the specific need. The theory of operation of all types are very similar, and complete mastery of one will enable you to distinguish and understand individual differences.

Identification of the three basic types is relatively simple. Figure 47-1 represents a basic Astable, figure 47-2 a Monostable, and figure 47-3 a Bistable multivibrator. The output waveshapes of each are shown, along with the input trigger if a trigger is required. Use these schematic diagrams and waveshapes while reading the explanations that follow.

The names of the three basic multivibrators are derived from the number of stable states. For instance, the Astable has no stable state. Q1 and Q2 will alternately switch from cutoff to saturation. When Q1 is cutoff, feedback

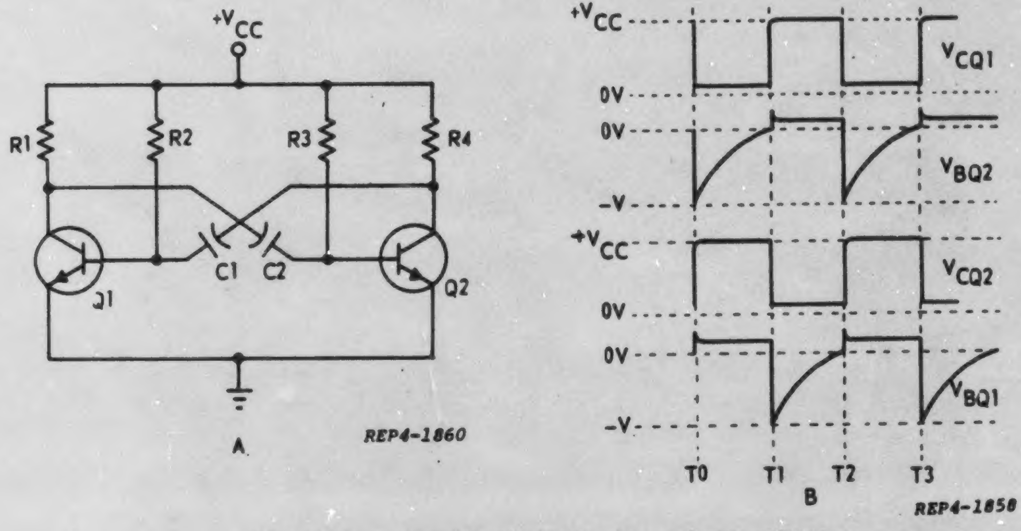


Figure 47-1. Astable Multivibrator and Waveshapes

causes Q2 to saturate. The Monostable has one stable state. Because of the bias arrangement, one transistor will remain cutoff (Q1 in figure 47-2), and the other will remain saturated until an external trigger is applied. The trigger will cause the cutoff transistor to saturate and the saturated transistor to cutoff. After a period, determined by the RC time constant (R2 and C2 of figure 47-2), the circuit will return to the original state until the next trigger is applied. The Bistable, as the name implies, has two stable states. One transistor will be saturated and the other transistor cutoff until an external trigger is applied. The trigger causes the transistors to reverse states, and remain in the reverse state until a second trigger is applied to switch them back.

For circuit identification, (figure 47-1) note that the astable circuit has a resistor/capacitor combination in each base circuit, C2/R3 for Q2, and C1/R2 for Q1. The monostable has a resistor/capacitor combination (figure 47-2) in only one base circuit (R2/C2 for Q2). The bistable uses direct coupling from the collector to base of both transistors (figure 47-3). In addition, the bistable employs an emitter resistor that is common to both transistors (R4).

The waveshapes of each type multivibrator are valuable aids to understanding their operational characteristics. For instance, the waveshapes of the Astable circuit show that Q1 is saturated (T0 to T1) while Q2 is cutoff. It also shows that Q2 is being held at cutoff by the negative signal on its base. Furthermore, it shows that the voltage on the Q2 base decreases at an exponential rate, and Q2 again becomes saturated when the voltage decreases sufficiently. C2 discharging through R3 determines how long Q2 stays cutoff. C1 discharging through R2 determines how long Q1 remains cutoff (T1 to T2). The cutoff time of Q2 added to the cutoff time of Q1 produces one complete cycle (T0 to T2). Therefore, the output PRF is controlled by the base RC components (R2, C1, R3, C2). The square wave can be taken from the collector of either transistor with 180 degrees phase relationship.

The astable multivibrator waveshapes are fairly straightforward, and if the location of one waveshape is given, the location of the other three can be determined. Note that both transistors are common emitter configurations, and a phase shift of 180 degrees will take place between the base and collector of each. Since the base circuits have RC time constants determining their waveshapes, they will have exponential curves. If you were given the waveshape for V_{BQ2}, you would know that V_{BQ2} is the same shape but 180 degrees out of phase. Other similar relationships exist among the waveshapes of the astable multivibrator.

The waveshapes for the monostable and bistable circuits are equally as simple to determine. You should note that the monostable circuit has an exponential base circuit waveform on only one transistor, and the bistable circuit has square waves throughout. In addition, the monostable circuit pulse width (T1 to T2) is controlled by the size of C2 and R2, but the output PRT (T1 to T3) is controlled by the input trigger. Both the pulse width (T1 to T2) and PRT (T1 to T3) of the bistable circuit is controlled by the input trigger. The bistable circuit takes two triggers to produce one cycle out, or it divides the input frequency by two.

Troubleshooting multivibrator circuits (see figure 47-4) is relatively simple if you remember the basic concepts of transistor amplifiers. For instance, you may recall that increasing forward bias on a transistor decreases the transistor's resistance and increases the current flowing through it. If the forward bias is increased enough, the transistor will become saturated, its resistance will be very low and the voltage from collector to ground (V_C) will almost drop to zero.

On the other hand, decreasing forward bias on a transistor increases its resistance and decreases the current through it. If the bias is decreased enough, a point is reached where it becomes reverse biased, and the transistor is cutoff. When cutoff is reached, resistance is maximum and current almost ceases to flow through it. At cutoff, the

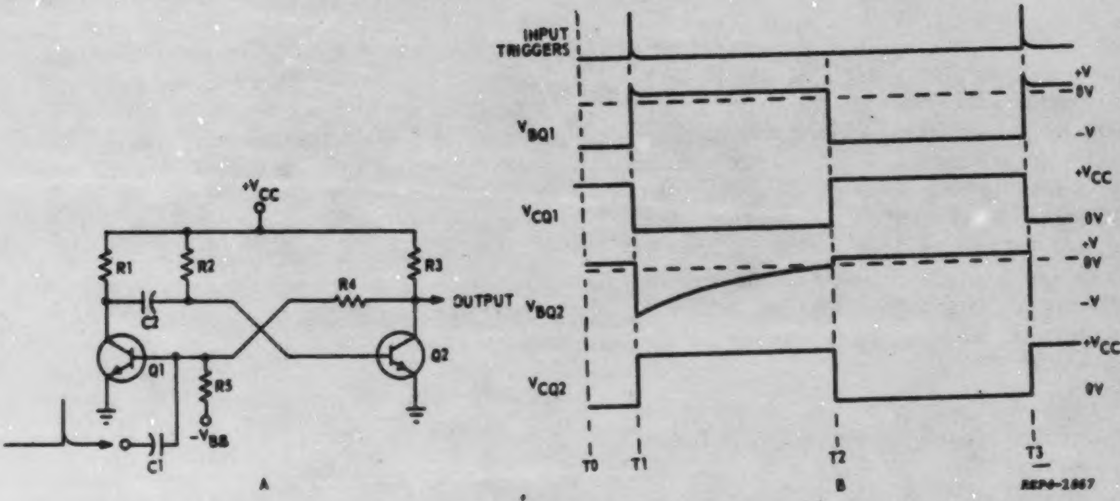

+VCC
R1
R2
R3
C2
R4
OUTPUT
Q1
Q2
R5
-VBB
C1
A
INPUT TRIGGERS
VBQ1
VCQ1
VBQ2
VCQ2
+V
0V
-V
+VCC
0V
+V
0V
-V
+VCC
0V
T0
T1
T2
T3
B
REP4-2067

Figure 47-2. Monostable Multivibrator Waveshape.

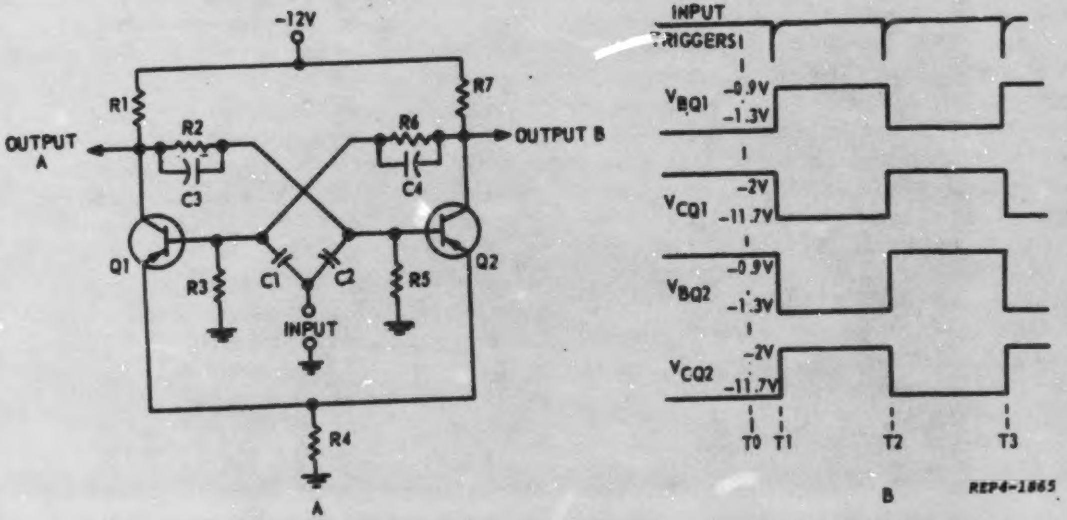

-12V
R1
R7
OUTPUT A
R2
R6
OUTPUT B
C3
C4
Q1
Q2
R3
C1
C2
R5
INPUT
R4
A
INPUT TRIGGERS
VBQ1
-0.9V
-1.3V
VCQ1
-2V
-11.7V
VBQ2
-0.9V
-1.3V
VCQ2
-2V
-11.7V
T0
T1
T2
T3
B
REP4-1865

Figure 47-3. Bistable Multivebrator and Waveshapes

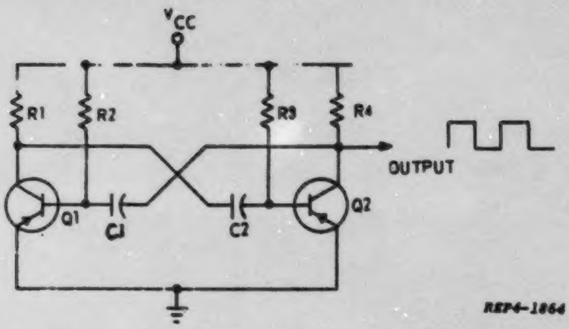


Figure 47-4. PNP Astable Multivibrator

collector to ground (V_C) voltage is nearly equal to V_{CC}.

Symptom: V_C of Q1 is nearly equal to V_{CC} and V_C of Q2 is very close to zero volts. (See figure 47-4).

Cause: The symptom indicates that Q1 is at cutoff and Q2 is saturated. What would cause this? One possibility is R2 open. To understand this, trace the forward bias current path for Q1 from $-V_{CC}$, through R2, the emitter/base junction to ground. With R2 open, Q1 would have no forward bias. It will be cutoff, and its collector voltage (V_C) would very nearly equal V_{CC}. V_{CC} would be coupled from Q1 collector to Q2 base causing it to saturate, and the collector to drop to a level close to zero.

Q1 open would also cause this symptom. Remember that applied voltage (in this case (V_{CC}) is dropped across an open. V_{CC} (from the collector of Q1) would be coupled to the base of Q2, keeping it saturated and its collector voltage nearly equal to zero volts.

Symptom: V_{CQ1} is nearly equal to zero volts, and V_{CQ2} is nearly equal to V_{CC}.

Cause: R3 open or Q2 open. If necessary, you can explain this to yourself by following the explanation for the symptom above, and substituting Q2 for Q1, Q1 for Q2, R3 for R2, and R2 for R3.

Symptom: V_{CQ1} equals zero volts. V_{CQ2} is very low but greater than zero volts.

Cause: R1 open or Q1 shorted would cause this symptom. R1 and Q1 are in series; and with R1 open, total voltage would be dropped across R1, leaving none to be dropped between the Q1 collector and ground. With Q1 shorted, its resistance would be zero ohms and would drop no voltage from collector to ground. How would this cause Q2 to be saturated and keep the collector voltage near zero volts? Recall that the only thing which will cause Q2 to decrease in conduction (and cutoff) is a changing voltage coupled to its base from the collector of Q1. Since the collector of Q1 is remaining at zero volts, C2 can not charge and discharge, and nothing is coupled from the Q1 collector to Q2 base. Therefore, since Q2 has a constant forward bias from $-V_{CC}$, through R3, the emitter/base junction to ground, it will conduct constantly near saturation.

Symptom: V_{CQ2} and V_{CQ1} is very low but greater than zero volts.

Cause: C1 open or C2 open. Assume that C1 is open for the following explanation. When power is first applied, both transistors initially conduct almost at saturation, and V_C of both will be low. With C1 open, nothing will be coupled from the collector of Q2 to the base of Q1. V_C of Q1 will stabilize at a value determined solely by the amount of forward bias current that flows through R2 and the emitter/base junction. Since V_C of Q1 will not be changing, nothing will be coupled to the base of Q2. Therefore, V_{CQ2} will be determined solely by the forward bias current that flows through R3 and the emitter/base junction. Since the value of R2 and R3 is chosen to cause the transistors to conduct near saturation, V_C of both will be very low. By substituting C2 for C1 and Q2 for Q1, you can go through the same explanation for C2 open.

Symptom: V_{CQ1} equals V_{CC}; V_{CQ2} nearly equals zero volts.

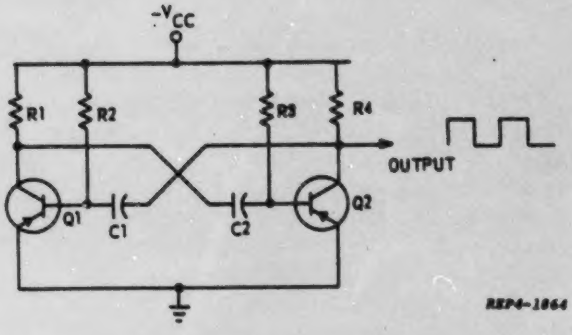


Figure 47-4. PNP Astable Multivibrator

Cause: R1 is shorted. Recall that no voltage is dropped across a shorted component (R1 in this case), and since R1 and Q1 are in series, V_{CC} would be measured on the Q1 collector. This voltage is coupled to the base of Q2 causing it to saturate, and its collector voltage nearly equal to zero volts.

Symptom: V_{CQ2} equals V_{CC}; V_{CQ1} nearly equals zero volts.

Cause: R4 shorted. You can explain this malfunction by following the preceding explanation, substituting R4 for R1, Q2 for Q1, and Q1 for Q2.

Before discussing the following malfunctions, a brief review is in order. Recall that increasing forward bias of a transistor beyond a given point (depending on the transistor's characteristics) will cause structural breakdown and destruction of the transistor. In all probability, structural breakdown would occur if any one of the base components (C1 and R2 for Q1, and C2 and R3 for Q2) is shorted. In the following discussions you can assume that the transistors can stand the added current without structural breakdown.

Symptom: V_{CQ1} and V_{CQ2} nearly equal to zero.

Cause: C1, C2, R2, or R3 is shorted. You should see that parallel paths now exist for forward bias current (from $-V_{CC}$ through R2 and from $-V_{CC}$ through R4 and around the shorted C1). These two currents combine as the base/emitter current for Q1, causing V_{CQ1} to be very near zero. Since the voltage does not change, nothing is coupled to Q2 to affect its operation. R3 allows enough current to flow through the emitter/base junction of Q2 to cause saturation and its collector voltage will be near zero. Any of the other three base circuit components shorted will cause the same operation.

If you thoroughly understand the troubleshooting of the astable circuit as explained above, you should be able to apply this knowledge in troubleshooting the monostable and bistable circuits.

If the waveshape of a square wave signal becomes distorted or rounded, a Schmitt Trigger circuit may be used. This circuit will furnish a sharp rectangular output pulse of about the same duration and polarity as the input signal. The Schmitt Trigger restores a distorted square wave to its original shape.

The Schmitt trigger is basically a multivibrator. The main difference is that one of the coupling networks is replaced by a common emitter resistor, providing additional regenerative feedback to obtain a faster switching time. The circuit is shown in figure 47-5.

In the quiescent state, Q1 is cut off, and Q2 is held at saturation by the negative voltage developed by the voltage dividing network R3, R4, and R5. The current through Q2 causes a voltage drop across R7, reverse biasing Q1 and keeping it cut off. The output taken from the collector of Q2 is about 0 volts.

At T0, the negative signal applied to input A has sufficient amplitude to turn Q1 on. The collector of Q1 goes to about 0 volts

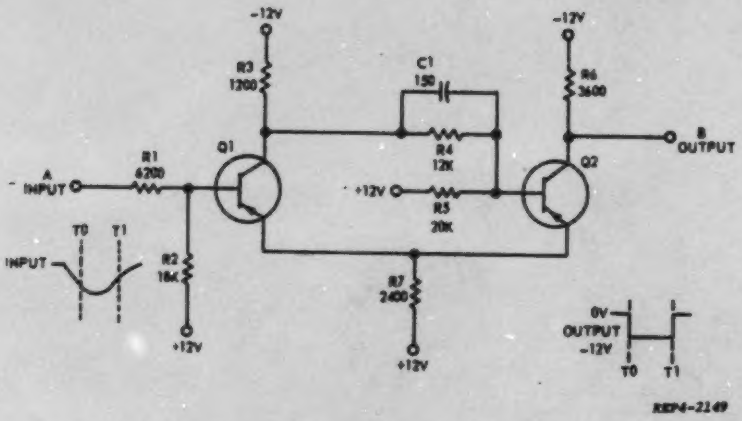


Figure 47-5. Schmitt Trigger

as the transistor conducts. This change in a positive direction is coupled to the base of Q2 causing a decrease in conduction. The decrease in conduction of Q2 further increases forward bias on Q1 until it saturates. With Q1 saturated Q2 will be cutoff and the output will be close to V_{CC}.

The circuit remains in this state until T1 when the input voltage becomes less negative. At this time, Q1 will start to conduct less and its collector voltage begins to change in a negative direction. This change is coupled to the base of Q2 which, in turn, reflects reverse bias on Q1 to cut it off. With the collector of Q1 at negative V_{CC}, Q2 conducts near saturation, and the output is near zero volts.

Notice how the rounded input wave is converted to a square wave output. The sharp rise and fall of the edges is due to the regenerative feedback between Q2 and Q1. Any slight change in the conduction of Q1 is applied to the base of Q2 which changes the emitter voltage of Q1. Capacitor C1 speeds the transition from one state to the other.

Schmitt trigger circuits are not only used for squaring circuits but also as voltage-level sensing circuits. Voltage sensing circuits are useful in warning or control circuitry. If the input voltage rises above or falls below a specified level, the Schmitt circuit produces an output, which activates a warning device.

Since the troubleshooting theory of the Schmitt trigger circuit is very similar to the astable multivibrator, the following symptoms and probable causes are presented without explanation. Refer to figure 47-5 while analyzing the troubles and causes.

Symptom: No output; V_{CQ2} is near zero.

Possible Causes: R3, R4, or C1 shorted; R6 open.

Symptom: V_{CQ2} is normal; no output.

Possible Causes: R1 or Q1 open; R2 shorted.

Symptom: High frequency distortion in output.

Possible Cause: C1 open.

Module 48

SOLID STATE SAWTOOTH GENERATORS

A sawtooth generator, as the name implies, generates an output signal shaped like the tooth of a saw. The deflection plates of an electrostatic deflection cathode ray tube, such as used in most oscilloscopes, requires a voltage of this shape for proper operation. Several methods, all involving the charge

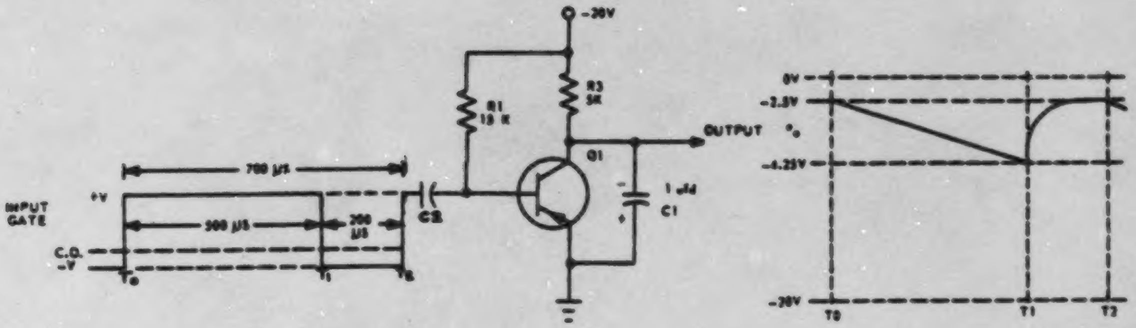


Figure 48-1. Sawtooth Generator

of a capacitor, are used in producing a signal of this shape. We will discuss only one of the most common solid state types.

The circuit and waveshapes shown in figure 48-1 should be used with the explanation that follows.

First, look at the schematic diagram and disregard the input signal. Q1 is biased very near saturation by the current flowing down from $-V_{CC}$, through R1, and through the base /emitter junction to ground. With Q1 biased near saturation, it effectively shorts C1 and a very small voltage (-2.5 volts, as shown on the output waveshape) will be dropped from collector to ground. Without an input signal, V_{CQ1} will remain at this level.

Apply the positive going input gate (T0 to T1) to the base of Q1. This positive going voltage applied to the N-type base reverse biases Q1, and causes it to cutoff. When Q1 cuts off V_{CQ1} cannot immediately jump to V_{CC} because C1 has to charge. Since the capacitance of C1 and resistance of R3 determines how fast C1 will charge, the V_{CQ1} will change at an exponential rate (T0 to T1 of the output signal). The charge time (slope) of the output wave is developed at this time. At T1 of the input gate, the base signal goes back in a negative direction, Q1 is again forward biased, and the V_C of Q1 returns to its original level (-2.5 V). This change does not occur instantly (as shown on the output signal) because C1 has to discharge. The discharge time is much less than the charge time, because the capacitor's discharge path contains the very small resistance of the saturated Q1. A complete cycle has been produced in the output. The PRF of the output is determined solely by the input gate. Observe that the slope portion (T0 to T1) of this output signal appears to be linear, which is most important.

You may recall that the first 10% of the charge on a capacitor is quite linear. You can prove this by checking the Universal Time Constant Chart handout given you earlier in this course. If the capacitor is allowed to charge to a level not exceeding 10% of applied voltage (.1 time constant), the sawtooth wave will be linear. From your experience with an oscilloscope, you should appreciate the need for sawtooth linearity.

The sawtooth voltage is applied to the deflection plates to move the electron beam across the oscilloscope face. If the sawtooth was not linear, then the signal produced on the oscilloscope face would not be linear. Consequently, in order that frequency can be measured accurately, the sawtooth wave must be very linear. It will be linear if the capacitor is not allowed to charge to more than 10% of applied voltage.

Now, how is the percent of charge controlled? In this circuit, it is controlled two ways. The input gate determines the cutoff and conduction time of Q1. It determines how long C1 will be allowed to charge. Linearity would be improved by shortening the cutoff time of Q1, and impaired by increasing the cutoff time of Q1. The values of C1 and R3 will determine how fast C1 will charge. Linearity can be assured by choosing values of capacitanco and resistance such that not more than .1 time constant elapses during the cutoff time of Q1. Increasing the size of either (or both) C1 or R3 would improve output linearity, while decreasing the size of either or both would impair linearity. Amplitude of the sawtooth could be increased by increasing V_{CC} without affecting linearity.

Troubleshooting from a practical standpoint of this solid state sawtooth generator is adequately covered in the laboratory exercise. However, a brief discussion of theoretical troubleshooting of this circuit is in order. Since the principles covered in the first two paragraphs of multivibrator troubleshooting applies, you may find it to your advantage to review Module 47 digest. Refer to figure 48-1 during the troubleshooting discussion.

Symptom: V_{CQ1} is very low and no sawtooth wave is generated.

Possible Causes:

1. Circuit producing input gate is inoperative. Without an input gate to cut Q1 off, it would remain saturated by the forward, bias current flowing through R1.

2. C2 open. Input gate signal would never reach base of Q1.

3. (Probable) R1 is shorted. Forward bias would be high enough in amplitude that input gate would not cause Q1 to cutoff.

4. C1 has low resistance, is shorted (leaky). A leaky capacitor acts like a resistor. And, if such were the case, C1 and R3 would form a simple resistive voltage divider. The V_{CQ1} would depend upon the ohmic resistance that C1 had.

Symptom: V_{CQ1} is zero volts.

Possible Causes:

1. Q1 or C1 is shorted. (Self-explanatory)

2. R3 open. An open R3 would drop all of V_{CC}, leaving none to be dropped from Q1 collector to ground.

Symptom: Output signal is an amplified version of the input gate, but 180 degrees out of phase.

Possible Causes: C1 open. Without C1 the circuit would be a simple common emitter amplifier.

Symptom: V_{CQ1} very nearly equals V_{CC}: no sawtooth wave is generated.

Possible Causes:

1. R1 open. No forward bias. Q1 cutoff, dropping most of V_{CC}.

2. Q1 open. C1 would charge to V_{CC} and remain charged, regardless of the input gate.

Module 49

SOLID STATE TRAPEZOIDAL GENERATORS

A common solid state trapezoidal generator, with input and output waveshapes is shown in figure 49-1. Use this schematic and the waveshapes while reading the following explanation.

The only difference between this circuit and that of a sawtooth wave generator is the addition of R3 in series with C2 between the collector and ground. Without the input gate, Q1 is biased near saturation and V_{CQ1} is nearly zero volts. At T0, the input gate causes Q1 to cutoff and act like an open. The circuit between ground and V_{CC} with Q1 open consists of C2, R3, and R2. At the first instant, C2 acts as a short and

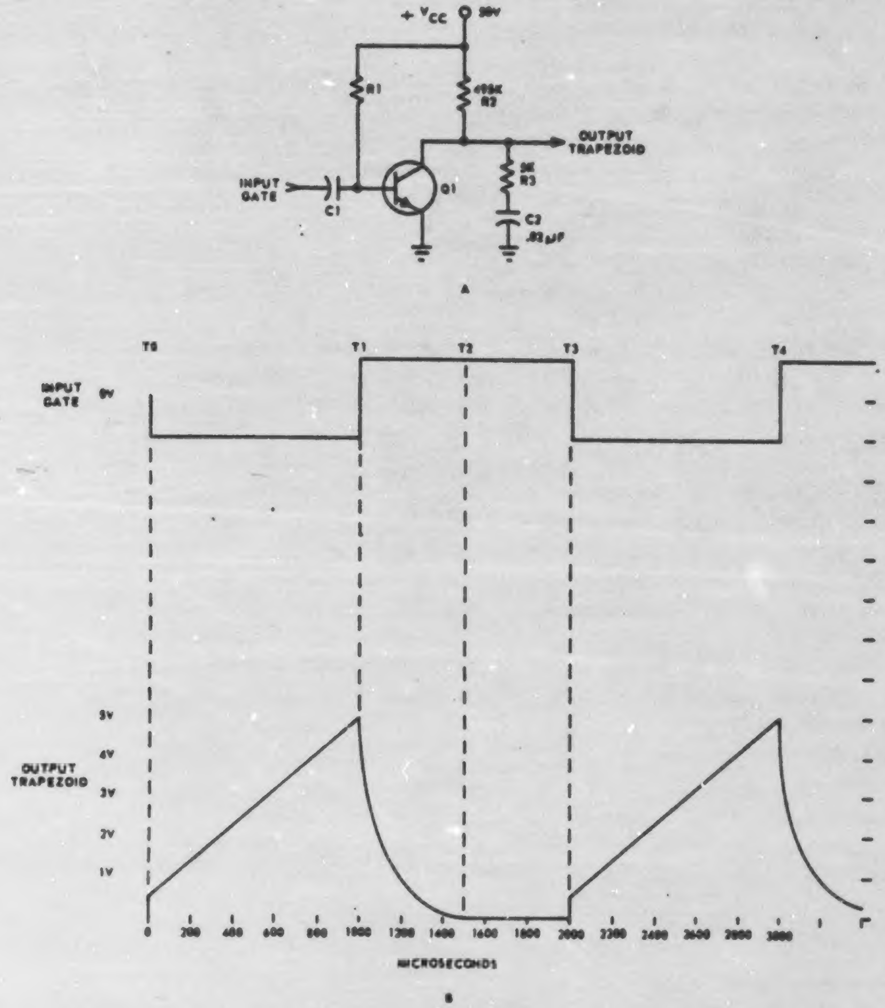

+ V_{CC}
30V
R1
499K
R2
OUTPUT
TRAPEZOID
INPUT
GATE
C1
Q1
3K
R3
C2
.02µF
A
T0
T1
T2
T3
T4
INPUT
GATE
0V
5V
4V
OUTPUT
TRAPEZOID
3V
2V
1V
0
200
400
600
800
1000
1200
1400
1600
1800
2000
2200
2400
2600
2800
3000
MICROSECONDS
B

Figure 49-1. Trapezodial Generator

50 volts V_{CC} will be dropped across R3 and R2. The voltage drop across R3 is what causes this circuit to produce a trapezoidal waveform. The R3 voltage drop is called jump voltage because V_{CQ1} "jumps" to this value (.5 volts in this circuit) as soon as Q1 cuts off. The amount of V_{CC} and the relative size of R2 and R3 will determine the amplitude of the jump voltage.

From this point forward, the trapezoidal wave generator functions exactly like the sawtooth wave generator you have just studied.

MODULE 50
SOLID STATE
LIMITERS AND CLAMPERS

Common diode limiters are divided into two major categories, series and shunt. As the names imply, the diode of the series limiter is in series with the load, and the diode of the shunt limiter is in parallel with the load. Both types can be used to limit either the positive or negative portion of the input signal. A positive limiter removes all or a portion of the positive half of the input signal, while a negative limiter removes all or a part of the negative half of the input signal. Shunt limiters often have fixed bias applied to the diode. When the diode is biased, the bias amplitude will determine the level of limiting.

Zener diodes are many times used as limiters. The Zener diode is connected in shunt with the load. When the input signal causes it to be forward biased, the zener will act like a regular diode. It will continue to operate without damage when the input reverses polarity, and if the signal exceeds the breakdown point, it will limit the output. The zener diode can be used to give the same effect as biased shunt diode limiters without the necessity of using a battery.

Transistors are also used for limiting applications. With a small forward bias, the input signal will cause a transistor amplifier to go into cutoff. With a relatively high forward bias, the input signal can cause the amplifier to go into saturation. In either case, a portion of the output signal would be clipped off (limited).

Increased forward bias would decrease cutoff limiting and increase saturation limiting. Decreasing forward bias would have the opposite effect. If the input signal amplitude were high enough, the transistor amplifier would be alternately driven to cutoff and saturation. In this case, both the negative and positive alternations would be limited in the output, and the circuit would be called an overdriven limiter.

Unlike limiters, the purpose of a clamper is not to alter the input signal shape, but to change the voltage level of either the upper or lower limits of the output signal. Clampers are like limiters since they are either positive or negative. A positive clamper clamps the upper extremity of the output signal. Without bias, the lower and upper reference level for positive and negative clamper is zero volts. With bias, the limits are determined by the bias voltage polarity and amplitude.

NOTES

ATC GP 3AQR3X020-X
Prepared by Keesler TTC
KEP-GP-42

Technical Training

Electronic Principles (Modular Self-Paced)

Module 42

PRINCIPLES OF OSCILLATIONS

March 1976

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March 1976

ELECTRONIC PRINCIPLES (MODULAR SELF-PACED)

MODULE 42

PRINCIPLES OF OSCILLATIONS

This Guidance Package is designed to guide you through this module of the Electronic Principles Course. This Guidance Package contains specific information, including references to other resources you may study, enabling you to satisfy the learning objectives.

CONTENTS

Title	Page
Overview	1
List of Resources	1
Adjunct Guide	1
Module Self-Check	2
Answers	4

OVERVIEW

1. SCOPE: There are three requirements for producing and maintaining a sine wave signal at a particular frequency. In this module, you will become familiar with these requirements. Also, you will learn to recognize the presence or absence of these three requirements in a simple block diagram of an oscillator.

2. OBJECTIVE: Upon completion of this module you should be able to satisfy the following objective:

From a list of statements, select the statement(s) that describe(s) the requirements for sustaining oscillations at a particular frequency.

LIST OF RESOURCES

To satisfy the objectives of this module, you may choose, according to your training, experience and preferences, any or all of the following.

READING MATERIALS:

Digest

Adjunct Guide with Student Text VI

AUDIOVISUALS:

Television Lesson 30-513, Characteristics of Crystals

Television Lesson 30-536, Introduction to LC Oscillators

AT THIS POINT, IF YOU FEEL THAT THROUGH PREVIOUS EXPERIENCE OR TRAINING YOU ARE FAMILIAR WITH THIS SUBJECT, YOU MAY TAKE THE MODULE SELF-CHECK.

CONSULT YOUR INSTRUCTOR IF YOU NEED HELP.

Supersedes KEP-GP-42, dated 1 August 1975.

ADJUNCT GUIDE

INSTRUCTIONS:

Study the referenced materials as directed.

Return to this guide and answer the questions.

Confirm your answers against the answers at the back of this Guidance Package.

Contact your instructor if you experience any difficulty.

Begin the program.

It is extremely difficult to pinpoint any particular area of electronics that does not require generation of a signal of some type. For instance, the HEART of every radio and television station transmitter is a type of signal generator called an oscillator. Since the use of signal generating circuits is so universal, it is imperative that you completely understand the principles involved in creating and controlling electronic signals. This module is designed to aid you in understanding these principles.

A. Turn to Student Text, Volume VI, and read paragraphs 1-1 through 1-67. Return to this page and answer the following questions.

1. The ideal sinusoidal oscillator produces a

__a. square wave output of constant frequency and amplitude.

__b. sine wave output of constant frequency and amplitude.

__c. square wave output of varying frequency and constant amplitude.

__d. sine wave output of varying frequency and constant amplitude.

2. The basic requirements for sustaining oscillations at a particular frequency are a/an

__a. frequency determining device, regenerative feedback, and a power supply.

__b. power supply, amplifier, and frequency determining device.

__c. amplifier, degenerative feedback, and a frequency determining device.

__d. frequency determining device, amplifier, and regenerative feedback.

3. Three common methods of frequency determination are through the use of

__a. class C amplifiers, class B amplifiers, and class A amplifiers.

__b. crystals, RC networks, and LC tank circuits.

__c. common emitter amplifiers, common collector amplifiers, and common base amplifiers.

__d. transformer coupling, RC coupling, and direct coupling.

4. In general, LC tank circuits (are) (are not) used to produce an audio signal, because the physical size of inductors and capacitors required to produce an audio frequency is extremely (large) (small).

5. The input signal to a sinusoidal oscillator is a (regenerative) (degenerative) feedback from the oscillator's output.

6. The two stability requirements of oscillators are ____________ and ____________.

7. A radio frequency oscillator requiring a high degree of frequency stability would most likely be designed with a/an (RC network) (crystal) (LC tank circuit) as the frequency determining device.

8. Increasing the load on an oscillator means that the resistance of the load has (increased) (decreased).

9. Increasing the load on an oscillator (improves) (impairs) frequency stability and (improves) (impairs) amplitude stability.

10. In general, an LC oscillator can be operated class

__a. A only.

__b. B only.

__c. C only.

__d. A, B, or C.

11. A square or rectangular waveform is produced by a transistor alternating between

______________ and ______________.

12. To produce a good square or rectangular wave, a transistor switch time must be (fast) (slow).

13. The first 10 percent of a capacitor's charge is used to form a sawtooth waveform because it is the (least) (most) linear.

14. The primary difference between a sawtooth and a trapezoidal waveshape is

______________.

CONFIRM YOUR ANSWERS

YOU MAY STUDY ANOTHER RESOURCE OR TAKE THE MODULE SELF-CHECK.

MODULE SELF-CHECK

QUESTIONS:

1. What are the three requirements for sustaining oscillations at a particular frequency?

__a. Overdriven amplifier, degenerative feedback, and a frequency determining device.

__b. Frequency determining device, amplification, and regenerative feedback.

__c. Power source, amplifier, and regenerative feedback.

__d. Amplifier, regenerative feedback, and an output coupling device.

2. The frequency of an oscillator that uses an LC tank circuit as the frequency determining device can be increased by

__a. increasing capacitance or increasing inductance.

__b. increasing capacitance or decreasing inductance.

__c. decreasing capacitance or decreasing inductance.

__d. decreasing capacitance or increasing inductance.

3. Amplitude stability and frequency stability of an oscillator are improved when the

__a. load impedance is increased.

__b. load impedance is decreased.

__c. frequency is increased.

__d. frequency is decreased.

CONFIRM YOUR ANSWERS

ANSWERS TO A:

1. b
2. d
3. b
4. are not, large
5. regenerative
6. frequency and amplitude
7. crystal
8. decreased
9. impairs, impairs
10. d
11. saturation and cutoff
12. fast
13. most linear
14. the jump voltage

If you missed ANY questions, review the material before you continue.

ANSWERS TO MODULE SELF-CHECK:

1. b
2. c
3. a

HAVE YOU ANSWERED ALL OF THE QUESTIONS CORRECTLY? IF NOT, REVIEW THE MATERIAL OR STUDY ANOTHER RESOURCE UNTIL YOU CAN ANSWER ALL QUESTIONS CORRECTLY. IF YOU HAVE, CONSULT YOUR INSTRUCTOR FOR FURTHER GUIDANCE.

NOTES

ATC GP 3AQR3X020-X

Prepared by Keesler TTC
KEP-GP-43

Technical Training

Electronic Principles (Modular Self-Paced)

Module 43

SOLID STATE LC OSCILLATORS

January 1976

AIR TRAINING COMMAND

7-10

Designed For ATC Course Use

ATC Keesler 6-3230

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Radar Principles Branch
Keesler Air Force Base, Mississippi

ATC GP 3AQR3X020-X
KEP-GP-43
January 1976

ELECTRONIC PRINCIPLES (MODULAR SELF-PACED)

MODULE 43

SOLID STATE LC OSCILLATORS

This Guidance Package is designed to guide you through this module of the Electronic Principles Course. This Guidance Package contains specific information, including references to other resources you may study, enabling you to satisfy the learning objectives.

CONTENTS

Title	Page
Overview	1
List of Resources	1
Adjunct Guide	1
Laboratory Exercise 43-1	6
Module Self-Check	9
Answers	12

OVERVIEW

1. SCOPE: It is intended in this module of instruction that you gain an understanding of the principles involved in producing sine wave signals. You will study several different methods, each utilizing the same basic principles of producing sine wave signals. You should learn that the type of oscillator used for a particular job is determined by the requirements, to include power, frequency, and stability. Finally, try to become proficient in the use of the oscilloscope as an aid in circuit checking and troubleshooting.

2. OBJECTIVES: Upon completion of this module you should be able to satisfy the following objectives.

a. From a schematic diagram of any one of the following oscillator circuits, select the components that comprise the feedback loop, frequency determining device, forward bias network, and frequency adjustment: Series Hartley; Shunt Hartley; Colpitts; Clapp; Butler.

b. Given a list of statements, select the statement(s) which describe(s) the effect of varying the output load on an LC tank circuit.

c. Given a list of statements, select the statement(s) which describe(s) the purpose of a buffer amplifier.

d. Given a trainer, multimeter, and oscilloscope, measure the change in output amplitude and frequency for a given change in load at the output of an LC oscillator circuit within ±10 percent accuracy.

e. Given a trainer, multimeter, and oscilloscope, measure the change in output amplitude and frequency between a maximum and minimum load with a buffer amplifier inserted between LC oscillator output and the load within ±10 percent accuracy.

Supersedes KEP-GP-43, 1 September 1975. Present stock will be used.

LIST OF RESOURCES

To satisfy the objectives of this module, you may choose, according to your training, experience, and preferences, any or all of the following.

READING MATERIALS:

Digest

Adjunct Guide with Student Text VI

AUDIOVISUALS:

Television Lesson 30-556, Oscillators, TSTR Hartley, Colpitts, and EOC

LABORATORY EXERCISE:

Laboratory Exercise 43-1, Solid State LC Oscillators

AT THIS POINT, IF YOU FEEL THAT THROUGH PREVIOUS EXPERIENCE OR TRAINING YOU ARE FAMILIAR WITH THIS SUBJECT, YOU MAY TAKE THE MODULE SELF-CHECK.

CONSULT YOUR INSTRUCTOR IF YOU NEED HELP.

ADJUNCT GUIDE

INSTRUCTIONS:

Study the referenced materials as directed.

Return to this guide and answer the questions.

Check your answers against the answers at the back of this Guidance Package.

Contact your instructor if you experience difficulty.

Begin the program.

Regardless of your particular Air Force Specialty Code in Electronics, you will see, operate, troubleshoot, and repair Air Force weapon systems containing oscillators. You learned in the previous module that one of the most common methods of producing and controlling a radio frequency sine wave signal is through the use of LC tank circuits. Just as there is a number of motor vehicles-all using basically the same type of engine-manufactured for different jobs, there is also a number of different oscillators, using basically the same type of frequency determining device and designed for different applications in electronics.

It is not the purpose of this module to teach you every detail about every LC oscillator in existence. However, the principles of several types are covered, and by applying the principles learned here, you will be able to analyze and troubleshoot all LC oscillators, regardless of how they have been modified.

A. Turn to Student Text, Volume VI, and study paragraphs 2-1 through 2-17. Return to this page and complete the following statement:

1. The three requirements for sustaining oscillations at a given frequency are:

a. ______________________

b. ______________________

c. ______________________

CONFIRM YOUR ANSWERS AT THE BACK OF THIS GUIDANCE PACKAGE.

B. Turn to Student Text, Volume VI, and study paragraphs 2-18 through 2-50. Return to this page and complete the following statements:

(NOTE: Questions 1 through 15 refer to the schematic diagram, figure 43-1).

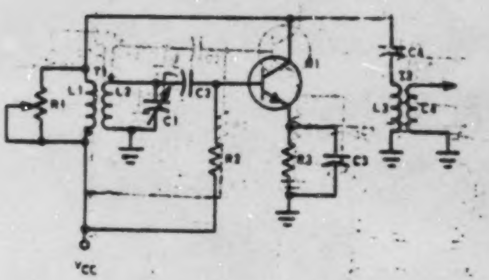


Figure 43-1

1. Figure 43-1 is the schematic diagram of a/an ________________ oscillator.

2. C1 and ____________ comprise the frequency-determining device. C1 is also used to adjust the ____________ of the oscillator.

3. R2 provides a path for, and controls the amount of ____________ current.

4. Increasing the resistance of R1 would cause ____________________ and output amplitude to increase.

5. T ________ and C ________ couple the feedback signal. T________ and C________ couple the output signal.

6. The purpose of R3 is to provide (forward bias) (temperature stability); C3 prevents (thermal runaway) (degeneration).

7. The regenerative feedback loop causes ______________ degrees phase shift. It is the combined effect of ________ degrees across Q1 and ________ degrees across T1.

8. Complete the following equations:

a. $V_{CC} = E_{R2} + E_{BE} + E_{R(\ )}$

b. $V_{CC} = V_{C(\ )} + E_{R(\ )} + E_{L(\ )}$

c. $V_{CE} = E_{L3} + E_{C(\ )} - E_{R(\ )}$

9. Shorting C4 would cause V_C to (decrease to near zero) (increase to near V_{CC}), and the circuit (would) (would not) oscillate.

10. Symptoms: V_C is nearly equal to V_{CC}; E_{R3} is near zero; E_{R2} is nearly equal to V_{CC}. A possible trouble is:

_____ a. R1 open

_____ b. R3 open

_____ c. R2 open

_____ d. L3 open

11. An open C2 (would) (would not) cause a significant change in V_C. A shorted C2 would cause V_C to be nearly equal to (zero) (V_{CC}).

12. An open C2 would cause the circuit to stop oscillating because the (feedback) (forward bias) path would be broken; a shorted C2 would cause the circuit to stop oscillating because the (feedback) (forward bias) would be eliminated.

13. Symptom: V_C is equal to V_{CC}. A possible trouble is:

_____ a. Q1 open.

_____ b. C4 shorted.

_____ c. T1 open.

_____ d. C3 shorted.

14. An open C4 (would) (would not) cause a significant change in V_C. The circuit (would) (would not) oscillate and an output signal (could) (could not) be detected across L4.

15. An open L1 (would) (would not) cause V_C to equal zero. It (would) (would not) break the feedback path, and the circuit (would) (would not) oscillate.

CONFIRM YOUR ANSWERS AT THE BACK OF THIS GUIDANCE PACKAGE.

C. Turn to Student Text, Volume VI, and study paragraphs 2-51 through 2-56. Return to this page and respond to the following statements/questions:

(NOTE: Question 1 through 5 refer to figure 43-2 schematic diagram.)

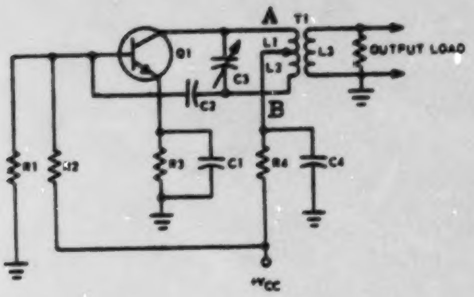


Figure 43-2

1. The identifying feature of the ______________________ oscillator is the tapped coil.

2. A path for direct current flow through the LC tank circuit denotes that the circuit is (series) (shunt) fed.

3. The purpose of C2 is to:

_____ a. prevent degeneration.

_____ b. shunt RF around the power supply.

_____ c. couple regenerative feedback.

_____ d. control oscillator frequency.

4. Moving the center tap of the primary of T1 toward point B would cause feedback amplitude to (increase) (decrease), output amplitude to (increase) (decrease), and (an increase) (a decrease) (no change) in output frequency.

5. The purpose of C4 is to (prevent degeneration) (shunt RF around the power supply).

CONFIRM YOUR ANSWERS AT THE BACK OF THIS GUIDANCE PACKAGE.

D. Turn to Student Text, Volume VI, and study paragraphs 2-57 through 2-59. Return to this page and respond to the following statements/questions:

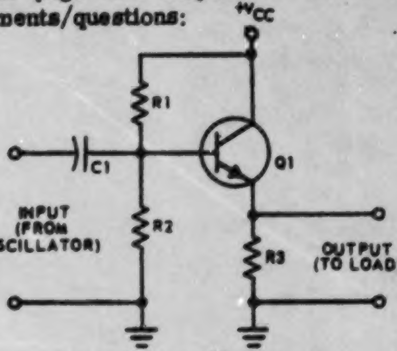


Figure 43-3

1. The correct name of the circuit of figure 43-3 is a ______________________ amplifier. Its purpose is to (provide a large voltage) (isolate the oscillator from load changes).

2. The common (base) (collector) (emitter) configuragion of the figure 43-3 circuit provides a (high) (low) input impedance, and the output load resistor can be selected to match the (input) (output) impedance of a circuit which follows it.

CONFIRM YOUR ANSWERS AT THE BACK OF THIS GUIDANCE PACKAGE.

E. Turn to Laboratory Exercise 43-1. This lab project will reinforce and prove most of the principles you have learned about LC oscillators. You will be able to observe the effect that a change in tank circuit capacitance has on oscillator frequency, the phase relationships that exist in the circuit, and the effect that a change in load has on frequency and amplitude stability.

In addition, you will gain valuable experience in using the oscilloscope to measure frequency and amplitude.

Return and continue with this program when the Laboratory Exercise has been completed.

F. Turn to Student Text, Volume VI, and study paragraphs 2-60 through 2-66. Return to this page and respond to the following statements/questions:

(NOTE: For questions 1 through 4 refer to the figure 43-4 schematic diagram.)

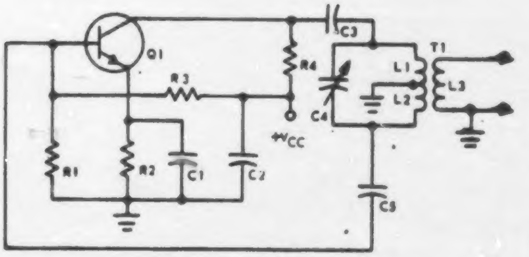


Figure 43-4

1. The tapped inductance and use of C3 to pass RF and block DC, identifies this circuit as a (series) (shunt) (Hartley) (Colpitts) oscillator.

2. The regenerative feedback path for this oscillator circuit includes Q1,

_____ a. R4, and R3.

_____ b. R4, C2, and R1.

_____ c. C3, T1, ground, and R1.

_____ d. C3, autotransformer (L1 & L2) and C5.

3. Complete the following equations:

a. $I_{R3} = I_B + I_{R(\ )}$

b. $I_{R4} = I_{R(\ )} - I_B$

c. $I_{R2} = I_B + I_{R(\ )}$

d. $I_B = I_{R3} - I_{R(\ )}$

4. Amplitude of the output signal is controlled by adjusting (C1) (T1 Tap position), and output frequency is controlled by adjusting (C4) (T1 tap position).

CONIFRM YOUR ANSWERS AT THE BACK OF THIS GUIDANCE PACKAGE

G. Turn to Student Text, Volume VI, and study paragraphs 2-67 through 2-78. Return to this page and respond to the following statements/questions:

(NOTE: For questions/statements 1 through 5, refer to figure 43-5 schematic diagram).

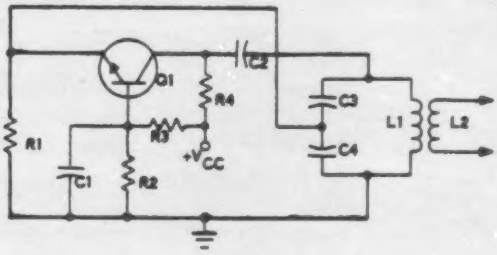


Figure 43-5

1. Obtaining regenerative feedback across a capacitive voltage divider identifies this circuit as a ________________ oscillator.

2. R ________ and R ________ form a voltage divider for developing forward bias.

3. In addition to developing the feedback signal, R1 also provides ________________ stabilization.

4. The collector load resistor is R ________.

5. One reason that the frequency stability of the Colpitts oscillator is very good is that C3 and C4 greatly reduce the effects of a change in ________________________.

(NOTE: For questions/statements 6 through 10, refer to the figure 43-6 schematic diagram).

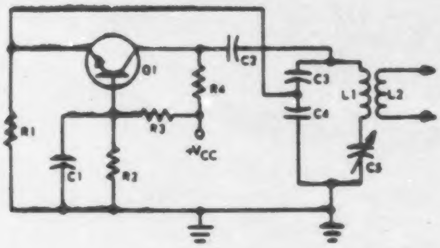


Figure 43-6

6. In this circuit, R3 provides a path for, and limits the amount of ________________ ________________ current.

7. The principal difference between the figure 43-5 and figure 43-6 schematic diagrams is the addition of ________________.

8. Symptoms: No output signal; V_C is normal. A possible trouble is:

______ a. C4 shorted.

______ b. C1 open.

______ c. C5 shorted.

______ d. C2 open.

9. Symptoms: No output signal; V_C is lower than normal; DC voltage on the emitter is zero. A possible trouble is:

______ a. C4 shorted.

______ b. C1 open.

______ c. C5 shorted.

______ d. C2 open.

10. Symptom: V_C equals 0 volts. A possible trouble is:

______ a. C1 shorted.

______ b. R3 open.

______ c. C4 shorted.

______ d. R4 open.

CONFIRM YOUR ANSWERS AT THE BACK OF THIS GUIDANCE PACKAGE.

H. Turn to Student Text, Volume VI, and study paragraphs 2-79 through 2-82. Return to this page and respond to the following statements/questions:

(NOTE: For questions 1 through 7, refer to the schematic diagram of figure 43-7).

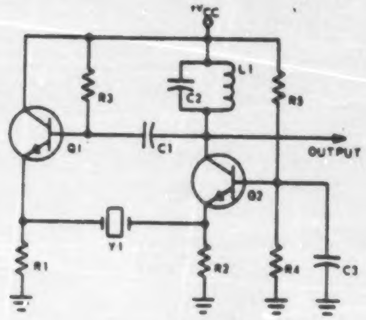


Figure 43-7

1. The regenerative feedback loop for this circuit is composed of:

______ a. R1, Y1, and R2.

______ b. Q1, Y1, Q2, and C1.

______ c. Q1, Y1, Q2, and the LC tank circuit.

______ d. Y1, Q2, R4, and R1.

2. Figure 43-7 is the schematic diagram of a ____________________ crystal oscillator.

3. The frequency determining device for this oscillator circuit is ____________________.

4. Quartz crystal Y1 in this circuit is operated in its (series) (parallel) resonant mode and offers (minimum) (maximum) impedance to its resonant frequency.

5. The load component for Q1 is (R3) (Y1) (R1), and the load component(s) for Q2 are (R2) (R5) (C2 and L1).

6. The purpose of C1 is to couple the (output) (feedback) signal.

7. R2 is required to develop the (input) (output) signal for Q2.

CONFIRM YOUR ANSWERS AT THE BACK OF THIS GUIDANCE PACKAGE.

LABORATORY EXERCISE 43-1

OBJECTIVES:

1. Given a trainer, multimeter, and oscilloscope, measure the change in output amplitude and frequency for a given change in load at the output of an LC oscillator circuit within ±10 percent accuracy.

2. Given a trainer, multimeter, and oscilloscope, measure the change in output amplitude and frequency between a maximum and minimum load with a buffer amplifier inserted between LC oscillator output and the load within ±10 percent accuracy.

EQUIPMENT:

1. Hartley Oscillator and Buffer Amplifier Trainer, DD6097
2. Oscilloscope
3. Multimeter
4. Transistor Circuit Power Supply, DD 4649

REFERENCE:

Student Text, Volume VI, paragraphs 2-52 through 2-59

CAUTION: OBSERVE BOTH PERSONNEL AND EQUIPMENT SAFETY RULES AT ALL TIMES. REMOVE WATCHES AND RINGS.

PROCEDURES:

1. Equipment preparation

a. Oscilloscope

controls	Position
VOLTS/CM	CH1 CH2

SEPARATE - CH1 & CH2	SEPARATE
CHOP-ALT	ALT
TIME/CM	.5 Microseconds
AC-GND-DC CH1 & CH2	AC
TRIG SELECT & LEVEL	EXT + AUTO
AC-ACF-DC	ACF
PULL X10 MAG	NORMAL (Push in)
POWER OFF	ON
CH1 & CH2 VERT POS	ON
INTENSITY AND FOCUS	Clear Presentation

b. Trainer

(1) C-103 to MAX CAP
(2) S-101 to Open Position
(3) R-109 fully counterclockwise

c. Power Supply

(1) Power on
(2) Adjust output to 6 volts (use built-in meter)

d. Interconnections

(1) Ground oscilloscope to trainer
(2) Connect power supply to trainer
(3) EXT TRIG input to TP-108
(4) CH1 to TP-103
(5) CH2 to TP-104

2. Trainer Analysis

This trainer incorporates a Series Hartley Oscillator, buffer amplifier, and a loading device (R-109). It is a simple practical method for you to use in learning the basic facts of a typical LC oscillator, including the effect that load changes have on amplitude and frequency stability.

3. Activity

a. Set the multimeter on DCV 20k ohms/V and 10 volt range. Connect the multimeter between TP-107 and ground. Readjust the transistorized power supply as necessary to obtain a reading of 6 volts.

b. Measure and record the amplitude of the signal on the collector and base of Q101.

Collector (TP-104) __________ Pk-Pk

Base (TP-103) __________ Pk-Pk

c. Measure and record the time for one cycle of the collector signal, and calculate the frequency ($f = 1/t$).

Time for 1 cycle __________ microseconds

Frequency __________ kHz

d. Fill in the blanks and underline the correct response to the following statements.

(1) Oscillator frequency is determined by C-__________, C-__________, and L-__________.

(2) The collector signal and the base signal are (in) (180° out of) phase, and the feedback is (regenerative)(degenerative).

e. Adjust C-103 to the MIN CAP position.

f. Measure and record the time for 1 cycle and calculate the frequency.

Time for 1 cycle __________ microseconds

Frequency __________ kHz

g. Underline the correct response in the following statement.

Decreasing the tank capacitance caused the time required for 1 cycle to (increase) (decrease) and the frequency to (increase) (decrease).

NOTE: Before continuing the exercise investigate the operation of the loading device. With R-109 adjusted fully counterclockwise the wiper arm is at the bottom of the resistor (ground) and the load has maximum resistance. As R-109 is adjusted clockwise the wiper arm moves up and the load resistance decreases.

h. Move S-101 to the left.

i. While observing the collector signal, rotate R-109 fully clockwise.

j. Rotate R-109 counterclockwise until the signal on the collector reappears.

k. Measure and record the amplitude of the collector signal.

Collector ____________________ Pk-Pk

l. Measure and record the time for 1 cycle, and calculate the frequency.

Time for 1 cycle__________ microseconds

Frequency ____________________ kHz

m. Underline the correct response to the following statements.

(1) As the load resistance decreased the oscillator load (increased)(decreased).

(2) (Increasing) (Decreasing) the load on an LC oscillator causes (a decrease) (an increase) (no change) in signal amplitude.

n. Turn R-109 fully clockwise. What effect does this have on the output signal?

____

____

____

o. Turn R-109 fully counterclockwise and move S-101 to the right.

p. While observing the collector signal, rotate R-109 fully clockwise.

q. Measure and record the amplitude of the collector signal.

Collector ____________________ Pk-Pk

r. Measure and record the time for 1 cycle, and calculate the frequency.

Time for 1 cycle__________ microseconds

Frequency ____________________ kHz

s. Underline the correct response to the following statements.

(1) The buffer amplifier causes the loading effect on the oscillator to be (more) (less).

(2) When a buffer amplifier is used as the stage following a typical LC oscillator the freuqency stability is (improved) (impaired), and the amplitude stability is (improved) (impaired).

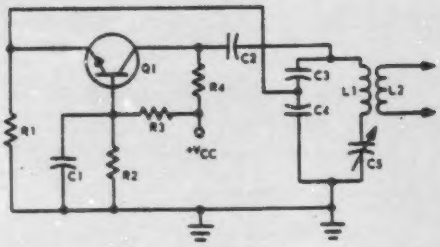
CONFIRM YOUR ANSWERS AT THE BACK OF THIS GUIDANCE PACKAGE.

MODULE SELF-CHECK

QUESTIONS:

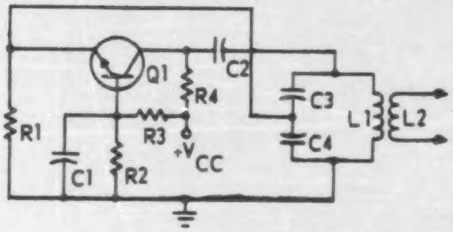
For questions 1 through 5 match the schematic diagrams (figures 43-8 through 43-12) to the oscillator names.

1. Series Hartley ____________________.
2. Shunt Hartley ____________________
3. Colpitts ____________________
4. Clapp ____________________
5. Butler Type Crystal ____________________.



Q1
C2
R4
C3
C4
L1
L2
R1
R3
+VCC
C1
R2
C5

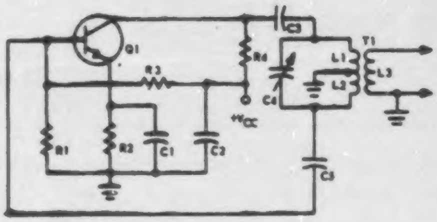
Figure 43-10



Q1
C2
R4
C3
L1
L2
R1
R3
+VCC
C4
C1
R2

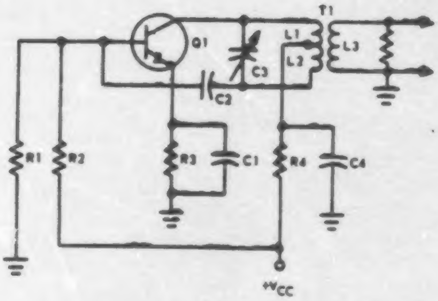
REP4-1421

Figure 43-8



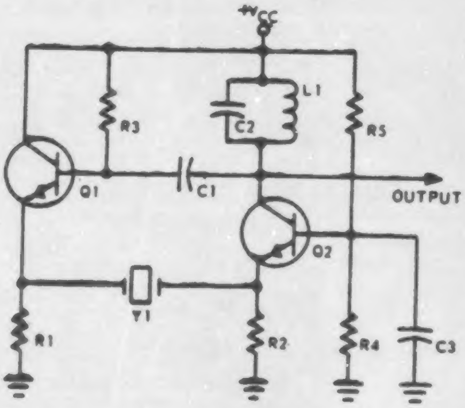
Q1
C3
R4
L1
T1
L3
L2
R3
C4
+VCC
R1
R2
C1
C2
C5

Figure 43-11



Q1
T1
L1
L3
L2
C3
C2
R1
R2
R3
C1
R4
C4
+VCC

Figure 43-9



+VCC
L1
C2
R3
R5
Q1
C1
OUTPUT
Q2
Y1
R1
R2
R4
C3

Figure 43-12

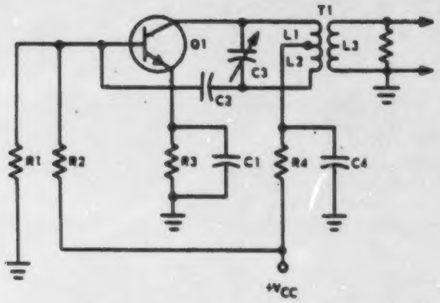


Figure 43-13

(Refer to figure 43-13 for questions 6 through 10.)

6. To increase the output frequency, you should decrease the value of ________.

7. The component used to couple a feedback signal from the output back to the input is

____

8. Symptoms: No output signal and V_C has increased. A possible trouble is

_____ a. C2 shorted.

_____ b. C2 open.

_____ c. R1 shorted.

_____ d. R1 open.

9. Symptoms: No output signal; V_C = Zero. A possible trouble is

_____ a. R4 open.

_____ b. C3 shorted.

_____ c. C2 shorted.

_____ d. R3 open.

10. An open R2 would cause

_____ a. V_C to decrease.

_____ b. I_C to increase.

_____ c. forward bias to increase to V_{CC}.

_____ d. forward bias to decrease to 0 volts.

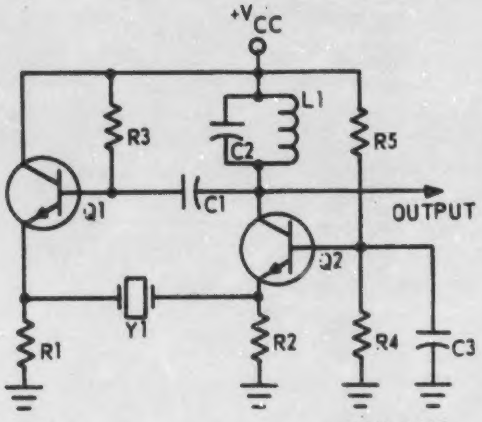


Figure 43-14

(For questions 11 through 13, refer to figure 43-14).

11. The component(s) that determine the frequency of this oscillator (is) (are) (Y1) (C2 and L1).

12. The primary purpose of R3 is to

_____ a. provide a feedback path from Q2 to Q1.

_____ b. establish and limit the forward bias for Q1.

_____ c. act as a load resistor for Q1.

_____ d. provide temperature stability.

13. The correct method of increasing the frequency of this oscillator is to

_____ a. decrease the value of C2.

_____ b. decrease the value of L1.

_____ c. replace Y1 with a thinner crystal.

_____ d. replace Y1 with a thicker crystal.

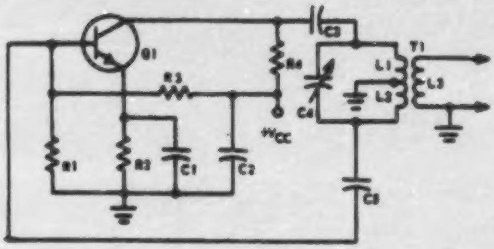


Figure 43-15

14. Refer to figure 43-15. The three purposes of autotransformer T1 are to act as a part of the FDD,

_____ a. determine feedback amplitude, and couple the output signal.

_____ b. couple the feedback signal, and determine amount of forward bias.

_____ c. determine amount of forward bias, and determine feedback amplitude.

_____ d. couple the feedback signal, and decouple RF from the power source.

15. Compared to an LC tank circuit, a crystal, used as the FDD of an oscillator circuit, will have a (higher) (lower) Q, and the frequency stability of the oscillator will be (improved) (impaired).

16. Refer to figure 43-16. Symptoms: No output and V_E is 0 volts. a possible trouble is

_____ a. R1 open.

_____ b. R4 open.

_____ c. C4 shorted.

_____ d. C2 shorted.

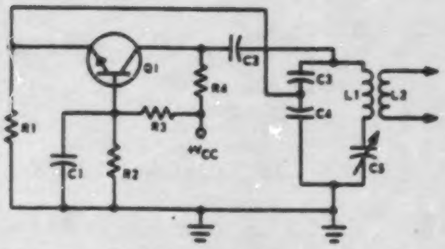


Figure 43-16

17. Refer to figure 43-16. The correct method of decreasing the frequency of this oscillator is to

_____ a. increase the capacitance of C5.

_____ b. decrease the capacitance of C5.

_____ c. increase the capacitance of C3 and C4.

_____ d. decrease the capacitance of C3 and C4.

18. Refer to figure 43-15. The components included in the feedback loop of this oscillator are Q1,

_____ a. R4, and R3.

_____ b. R4, C2, and R1.

_____ c. C3, L1, and R1.

_____ d. C3, FDD, and C5.

19. Refer to figure 43-16. Symptoms: V_C very high with no output. A possible trouble is

_____ a. Q1 shorted.

_____ b. Q1 open.

_____ c. C4 shorted.

_____ d. R2 open.

CONFIRM YOUR ANSWERS AT THE BACK OF THIS GUIDANCE PACKAGE.

ANSWERS TO A - ADJUNCT GUIDE

1. a. Amplification
   b. Frequency-determining device
   c. Regenerative feedback

If you missed ANY questions, review the referenced material before you continue.

ANSWERS TO B - ADJUNCT GUIDE

1. Armstrong
2. L2, frequency
3. Forward bias
4. feedback amplitude
5. T1 and C2; T2 and C4
6. temperature stability; degeneration
7. 360, 180, 180
8. a. $V_{CC} = E_{R2} + E_{BE} + E_{R3}$.

   b. $V_{CC} = V_{CE} + E_{R3} + E_{L1}$.

   c. $V_{CE} = E_{L3} + E_{C4} - E_{R3}$.
9. decrease to near zero, would not
10. c. R2 open.
11. would not; V_{CC}.
12. feedback, forward bias
13. a. Q1 open.
14. would not; would; could not
15. would not; would, would not

If you missed ANY questions, review the referenced material before you continue.

ANSWERS TO C - ADJUNCT GUIDE

1. Hartley
2. series
3. c. couple regenerative feedback
4. decrease, decrease, no change
5. shunt RF around the power supply

If you missed ANY questions, review the referenced material before you continue.

ANSWERS TO D - ADJUNCT GUIDE

1. buffer; isolate the oscillator from load changes.
2. collector, high, input

If you missed ANY questions, review the referenced material before you continue.

ANSWERS TO F - ADJUNCT GUIDE

1. shunt, Hartley
2. d. C3, autotransformer (L1 & L2) and C5
3. a. $I_{R3} = I_B + I_{R1}$.

   b. $I_{R4} = I_{R2} - I_B$.

   c. $I_{R2} = I_B + I_{R4}$.

   d. $I_B = I_{R3} - I_{R1}$.
4. T1 Tap Position, C4

If you missed ANY questions, review the referenced material before you continue.

ANSWERS TO G - ADJUNCT GUIDE

1. Colpitts
2. R2, R3
3. Emitter
4. R4
5. E-B capacitance
6. Forward bias
7. C5
8. d
9. a
10. d

If you missed ANY questions, review the referenced material before you continue.

ANSWERS TO H - ADJUNCT GUIDE

1. b. Q1, Y1, Q2, and C1.
2. Butler
3. Y1
4. series, minimum
5. R1, C2, and L1
6. feedback
7. input

If you missed ANY questions, review the referenced material before you continue.

ANSWERS TO LAB EXERCISE 43-1

3. Activity
    - b. Collector 3V to 5V Pk-Pk
      Base 1.4V to 2.8 Pk-Pk
    - c. Time for 1 cycle 2.5 to 3.2 microseconds
      Frequency 400 to 312 kHz
    - d. (1) C-102, C-103, L-101
      (2) 180° out of, regenerative
    - f. Time for 1 cycle 2.5 to 3 microseconds
      Frequency 400 to 333 kHz
    - g. Decrease, increase
    - k. Collector .8V to 2V Pk-Pk
    - l. Time for 1 cycle 2.75 to 3.3 microseconds
      Frequency 363 to 303
    - m. (1) increased
      (2) Increasing, a decrease
    - n. The oscillator load increased to the point where the circuit could no longer generate an AC signal.
    - q. Collector 3V to 5V Pk-Pk
    - r. Time for 1 cycle 2.6 to 2.8 microseconds
      Frequency 384 to 357 kHz
    - s. (1) less
      (2) improved, improved

If you missed ANY of the questions, or if there is more than 10% difference between your measurements and calculation and those listed above, go back and repeat that portion of the lab exercise. Consult the referenced material or the instructor for assistance, if required.

CONSULT YOUR INSTRUCTOR FOR THE PROGRESS CHECK.

ANSWERS TO MODULE SELF-CHECK

1.	Series Hartley	Figure 43- 9
2.	Shunt Hartley	Figure 43-11
3.	Colpitts	Figure 43- 8
4.	Clapp	Figure 43-10
5.	Butler Type Crystal	Figure 43-12

6. C3
7. C2
8. c. R1 shorted.
9. a. R4 open.
10. d. forward bias to decrease to 0 volts.
11. Y1
12. b. establish and limit the forward bias for Q1.
13. c. replace Y1 with a thinner crystal.
14. a. determine feedback amplitude, and couple the output signal.
15. higher, improved.
16 c. C4 shorted.
17. a. increase the capacitance of C5.
18. d. C3, FDD, and C5.
19. b. Q1 open.

HAVE YOU ANSWERED ALL OF THE QUESTIONS CORRECTLY? IF NOT, REVIEW THE MATERIAL OR STUDY ANOTHER RESOURCE UNTIL YOU CAN ANSWER ALL QUESTIONS CORRECTLY, CONSULT YOUR INSTRUCTOR FOR FURTHER INSTRUCTIONS.

166

PREPARE THE MAN

ATC GP 3AQR3X020-X
Prepared by Keesler TTC
KEP-GP-44

Technical Training

ELECTRONIC PRINCIPLES (MODULAR SELF-PACED)

MODULE 44

SOLID STATE RC OSCILLATORS

1 September 1974

AIR TRAINING COMMAND

7-10

Designed For ATC Course Use

DO NOT USE ON THE JOB

167

Basic and Applied Electronic Department
Keesler Air Force Base, Mississippi

ATC GP 3AQR3X020-X
KEP-GP-44
1 September 1974

ELECTRONIC PRINCIPLES
MODULE 44

This Guidance Package is designed to guide you through this module of the Electronics Principles Course. This Guidance Package contains specific information, including references to other resources you may study, enabling you to satsify the learning objectives.

CONTENTS

TITLE	PAGE
Overview	1
List of Resources	2
Digest	3
Adjunct Guide	7
Laboratory Exercise	13
Module Self-Check	19
Critique	23

Supersedes KEP-GP-44, 1 June 1974, which may be used.

168

SOLID STATE RC OSCILLATORS

1. SCOPE: Continuing your study of sine wave oscillators, in this module you will learn the principles involved in producing sine wave signals at low frequencies. Though two specific RC oscillators are discussed in the module, you should concern yourself more with the principles involved, rather than attempting to memorize the specifics of these two oscillators. In this way, you should be able to apply the principles learned to a specific circuit, regardless of how it has been modified to fit a particular need. Then, too, you will continue to build your ability to use the oscilloscope and multimeter as an aid in circuit checking and troubleshooting.

2. OBJECTIVES: Upon completion of this module you should be able to satisfy the following objectives:

a. From a schematic diagram of any one of the following oscillators, select the component(s) that comprise the feedback loop(s), frequency-determining device, forward bias network, output load, amplitude adjustment, and the frequency adjustment:

(1) Phase Shift.

(2) Wien Bridge.

b. Given a trainer, multimeter, and oscilloscope, measure the output amplitude and frequency of an RC oscillator circuit within ± 10 percent accuracy.

AT THIS POINT, YOU MAY TAKE THE MODULE SELF-CHECK .

IF YOU DECIDE NOT TO TAKE THE MODULE SELF-CHECK , TURN TO THE NEXT PAGE AND PREVIEW THE LIST OF RESOURCES. DO NOT HESITATE TO CONSULT YOUR INSTRUCTOR IF YOU HAVE ANY QUESTIONS.

177

LIST OF RESOURCES

SOLID STATE RC OSCILLATORS

To satisfy the objectives of this module, you may choose, according to your training, experience, and preferences, any or all of the following:

READING MATERIALS:

Digest

Adjunct Guide with Student Text

LABORATORY EXERCISE:

Laboratory Exercise 44-1

AUDIOVISUAL MATERIALS:

TV Lesson 30-517, Wein Bridge Oscillator, (11 minutes)

SELECT ONE OF THE RESOURCES AND BEGIN YOUR STUDY OR TAKE THE MODULE SELF-CHECK.

CONSULT YOUR INSTRUCTOR IF YOU REQUIRE ASSISTANCE.

SOLID STATE RC OSCILLATORS

During this discussion of RC oscillators, two types will be used. Figure 1 is called a Phase Shift oscillator; Figure 2 is a Wien Bridge oscillator.

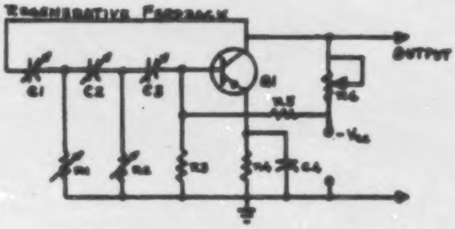


Figure 1

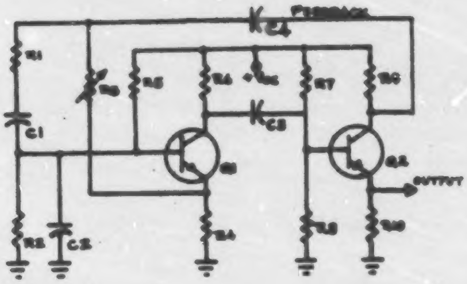


Figure 2

Both of these circuits have distinctive identifying features. The Figure 1 Phase Shift oscillator has three capacitors in series between the collector and base. The Wien Bridge oscillator uses two transistors. The load output and feedback output are taken from two different points, and it has both regenerative and degenerative feedback.

The forward bias arrangement for both of these oscillator circuits is identical to many other oscillator and amplifier circuits you have previously studied, and no detailed explanation will be offered here.

The frequency-determining devices for these oscillators, however, are not similar to those previously studied. First, the Phase Shift oscillator. You should recall from your study of RC time constants that a definite phase difference exists in the voltage developed across resistors and capacitors connected together in a circuit. You should also recall that the amount of phase difference across the capacitor and resistor will depend upon the value of resistance and capacitance and the frequency.

Take a look at the Figure 1 schematic diagram. Note that three RC networks (C1/R1; C2/R2; C3/R3) are in the feedback path between collector and base. A common emitter configuration amplifier circuit is used; therefore, any signal appearing at the base will be shifted 180 degrees at the collector. And, to have regenerative feedback, the signal must be shifted another 180 degrees between the collector and base. Since the phase shift across any one RC network is always less than 90 degrees, it is apparent that at least three RC networks must be used to obtain a phase shift of 180 degrees. And since frequency is one of the determinants of the amount of phase shift that will occur across any RC combination, it should also be apparent that any particular combination of three RC networks will produce a shift of 180 degrees at only one frequency. Therefore, only one frequency will be shifted in phase the right amount between collector and base to be a regenerative feedback. This will be the frequency at which the oscillator will operate. But, what if a need exists to change the frequency?

The value of capacitance and resistance in the RC networks also determines the amount of phase shift. And, if the capacitance of any capacitor in the phase shift network, or the resistance of any resistor, is changed, the frequency that will produce a 180 degree phase shift will also change. So, changing the value of either of these components will change the frequency that will be regenerative, and will change the operating frequency of the oscillator. C1, C2, C3, R1, and R2 are shown as being variable in the Figure 1 circuit, and varying either or all of them would cause a change in frequency. Remember that R3 is also a part of the frequency-determining device, but it is not shown as variable. You should see that R3 is also a part of the forward bias voltage divider network, and it should not be varied because a change in its resistance would also change the forward bias and amplification factor of the transistor. In fact, it is doubtful that you will ever see a Phase Shift oscillator in use that will have all of the components variable, as shown in Figure 1. It is done here so that you will realize that it is possible to change frequency by changing either of the component values in the feedback loop. Now that you see how the frequency can be changed, what about the amplitude?

In your study of amplifiers, you learned that changing the value of the collector load resistor would change the amplifier's amplification factor, and, therefore, the amplitude of the output. Note that R6, the collector load resistor, is variable. By changing the value of this resistor, the amplification factor of Q1 is changed. In addition, the amount of feedback will be changed, thereby changing the output amplitude. Now, to the Wien Bridge Oscillator.

Reflect for a moment on your previous study of feedback in amplifiers. Now, look at the Figure 2 schematic diagram. Starting with the collector for Q1, trace a signal path through C3 to the base of Q2. From the collector of Q2, trace the signal through C4. After C4, note that the signal has two paths to follow; one is through R3 to the emitter of Q1; the other is through R1 and C1 to the base of Q1. Now, for explanation, let's consider that when power was first applied to the circuit, the noise developed on the base of Q1 was going in a positive direction.

The positive-going voltage on the base of Q1 will be negative-going on the collector of Q1 and the base of Q2. Q2 will cause another 180 degree phase shift and the signal will be applied through C4, R1, and C1, back to the base of Q1 in a positive-going direction, and is regenerative feedback. Note that this regenerative feedback is developed across the combination of R2 and C2 in parallel. Note also that this signal is applied through R1 and C1 in series. Recalling your previous study of RC circuits, it should be apparent that maximum voltage will be developed on the base of Q1 at only one frequency. The amplitude will decrease when the frequency is raised because of the decreased X_C of C2. Amplitude will decrease at lower frequencies because of the increased X_C of C2. Amplitude will decrease at lower frequencies because of the increased X_C of C1. Curve "B" on Chart 1 represents the regenerative feedback. This illustrates, then, that the regenerative feedback loop is frequency selective. Therefore, R1, C1, R2, and C2 comprise the frequency-determining device. Now, for the degenerative feedback.

Look back at the Figure 2 schematic diagram, and locate the junction between R1 and C4. Recall from the previous paragraph that the signal along this line was re-applied to the base of

Q1 in a positive-going direction. Now, follow from this junction through R3 and note that the signal is developed across R4 and applied to the emitter of Q1. Note also that no reactive components are used in developing this voltage applied to the emitter; therefore, the amplitude of the signal developed will be the same regardless of the frequency. Line "A" on the chart below represents the degenerative feedback. But, why use both regenerative and degenerative feedback when we know that an oscillator requires regenerative feedback in order to oscillate?

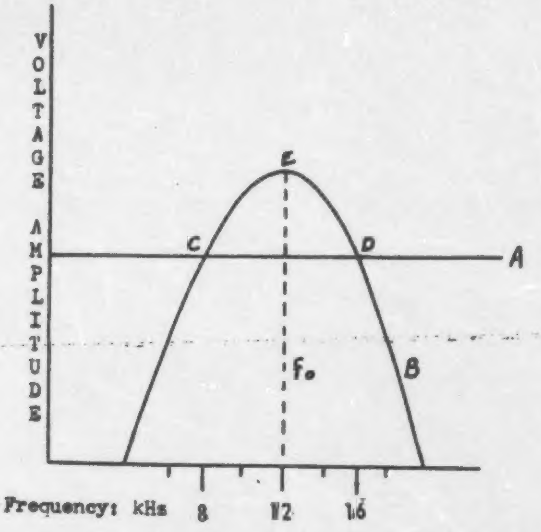


Chart 1

Look at Chart 1. For a moment, disregard line "A," representing degenerative feedback. Let each small division along the frequency line represent 2 kHz. Note that the center frequency is 12 kHz. Now, without the degenerative feedback, the half power points for curve "B" would be around 7 kHz and 17 kHz, and the oscillator could possibly oscillate at any frequency between these two points. Is this good frequency stability? NO.

Now, take another look at Chart 1 with line "A" in place. Curve "B" really does not exist below points "C" and "D" because it is cancelled out by the degenerative feedback, line "A." And, considering points "C" and "D" as the zero volts amplitude for regenerative feedback, the half power points of curve "B" have been moved to approximately 11 kHz and 13 kHz. It should be apparent that the frequency stability has been greatly improved. This, then, is the purpose of using both regenerative and degenerative feedback -- to improve frequency stability. How can the output amplitude and frequency be changed?

Variable resistor R3 controls the amount of degenerative feedback applied to the emitter of Q1. With this in mind, again consider Chart 1. If the degenerative feedback were adjusted so that its amplitude was greater than the peak of the regenerative feedback, point "E," all of the regenerative feedback would be cancelled out and the circuit would not oscillate. On the other hand, decreasing the amplitude of degenerative feedback below the points "C" and "D" level would, in effect, increase the amount of regenerative feedback, causing a corresponding increase in output amplitude.

DIGEST

Frequency can be changed by changing the value of any component in the frequency-determining device. In this case, it would be R1, R2, C1, or C2. The usual method, however, is to either gang-tune C1 and C2, or gang-tune R1 and R2. Now, for some principles that are common to both the Phase Shift and Wien Bridge oscillators.

In order to produce a sine wave output, both the Phase Shift and Wien Bridge oscillators must be operated Class A. The reason for this is that neither circuit contains an LC tank circuit that will "ring" and produce a sine wave when only a small portion of a sine wave is applied to it.

For troubleshooting, refer to paragraph 2-91, Volume VI of the Student Text. Laboratory Exercise 44-1 will also illustrate the effects of certain malfunctions, and it will demonstrate the proper methods to use in measuring output amplitude and frequency.

YOU MAY STUDY ANOTHER RESOURCE OR TAKE THE MODULE SELF-CHECK.

SOLID STATE RC OSCILLATORS

INSTRUCTIONS:

Study the referenced materials as directed.

Return to this guide and answer the questions.

Check your answers against the answers at the top of the page following the questions.

If you experience any difficulty, contact your instructor.

Begin the program.

You have previously learned that an oscillator is an amplifier that has a portion of its output returned to its input in phase. You also learned that a method of frequency control -- keeping the frequency constant -- is necessary in a practical circuit. The LC tank circuit and quartz crystal are very practical methods for establishing and maintaining a particular frequency when the frequency is high. However, they are impractical in the audio range. The physical size of capacitors and inductors that would be required rules them out. And a quartz crystal, in order to oscillate at an audio frequency, would be relatively thick physically, and would require too much external power to extablish and maintain oscillations. These problems are solved by using resistor/capacitor (RC) networks as the frequency-determining device for audio oscillators.

A. Turn to Student Text, Volume VI, and study paragraphs 2-84 through 2-91. return to this page and answer the following statements/questions.

For questions 1 through 10, refer to the Figure 3 schematic diagram.

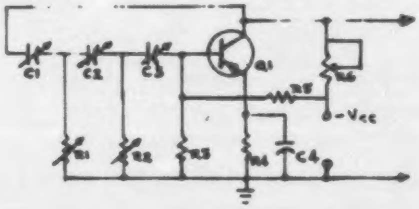


Figure 3

1. In the feedback loop for this circuit, starting with the base of Q1, the signal is shifted ______________ degrees; 180 degrees across Q1 and ______________ degrees across the RC networks.

2. C1 and R1 cause a phase shift of 54 degrees. In order to have regenerative feedback, it is necessary for the two remaining RC networks to shift the signal __________ degrees.

ADJUNCT GUIDE

3. Complete the following equations:

a. IR4 = IR6 + IR____ - IR ____.

b. $V_{CC} = V_C + ER$ ____ .

c. IR5 = IR_{BE} + IR ____.

4. The component that helps to determine both the frequency and forward bias of the Figure 3 oscillator circuit is ____________________ . .

5. Increasing the value of R6 would cause feedback amplitude to (increase) (decrease), and output amplitude to (increase) (decrease).

6. Symptoms: V_C is high, and there is no output. A possible trouble is:

______ a. C3 open.

______ b. C3 shorted.

______ c. C4 shorted.

______ d. C4 open.

7. Symptoms: Circuit is not oscillating; forward bias and V_C are normal. A possible trouble is:

______ a. C1 open.

______ b. C3 shorted.

______ c. C4 open.

______ d. C4 shorted.

8. Symptoms: V_C is zero volts and circuit is not oscillating. A possible trouble is:

______ a. R4 open.

______ b. R3 open.

______ c. R5 open.

______ d. R6 open.

9. The feedback loop is comprised of Q1, ________, ________, and ________ .

10. Symptoms: V_C very nearly equals V_{CC}; circuit is not oscillating. A possible trouble is:

_____ a. C3 shorted.

_____ b. C4 shorted.

_____ c. R3 open.

_____ d. R5 open.

CONFIRM YOUR ANSWERS ON THE NEXT EVEN NUMBERED PAGE.

B. Turn to Student Text, Volume VI, and study paragraphs 2-93 through 2-103. Return to this page and respond to the following statements/questions.

For questions 1 through 8, refer to the Figure 4 schematic diagram.

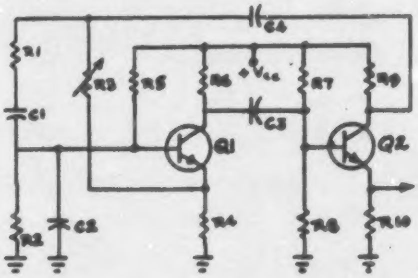


Figure 4

1. The Figure 4 circuit is correctly identified as a:

_____ a. Butler oscillator.

_____ b. Phase Shift oscillator.

_____ c. Wien Bridge oscillator.

_____ d. Colpitts oscillator.

2. Degenerative feedback is applied from Q2 back to the (base) (emitter) of Q1; degenerative feedback amplitude is controlled by _______________, and the degenerative feedback signal is developed across (R2 & C2) (R4).

3. The regenerative feedback amplitude in this circuit (is) (is not) affected by frequency, and degenerative feedback (is) (is not) affected by frequency.

ANSWERS TO A:

1. 360 degrees; 180 degrees
2. 126
3. a. $IR4 = IR6 + IR\underline{5} - IR\underline{3}$.
   b. b. $V_{CC} = V_C + ER\underline{6}$.
   c. $IR5 = IR_{BE} + IR\underline{3}$.
4. R3
5. increase, increase
6. b
7. a
8. d
9. C1, C2, and C3
10. d

If you missed ANY questions, review the material before you continue.

4. The components that comprise the complete frequency determining device for this circuit are:

_______a. R1 and C1.

_______b. R3 and C4.

_______c. R2 and C2.

_______d. R1, R2, C1, and C2.

5. The oscillator shown in Figure 4 must operate class ____________ in order to produce a sine wave output.

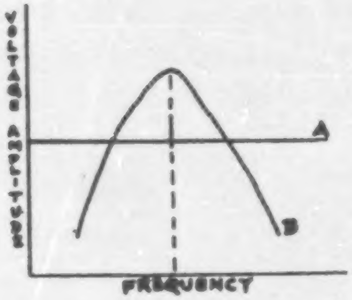


Figure 5

6. Given the diagram in Figure 5, line "A" represents (regenerative) (degenerative) feedback and curve "B" represents (regenerative) (degenerative) feedback.

7. Increasing the resistance of R3 would cause (an increase) (a decrease) (no change) in the amplitude of line "A" and (an increase) (a decrease) (no change) in the peak amplitude of curve "B."

8. From the following equations, select the one that correctly represents forward bias current for Q2.

______ a. I_{BE} = IR7 + IR8.

______ b. I_{BE} = IR7 - IR8.

______ c. I_{BE} = IR10 - IR7.

______ d. I_{BE} = IR9 + IR8.

CONFIRM YOUR ANSWERS ON THE NEXT EVEN NUMBERED PAGE.

C. Turn to Laboratory Exercise 44-1. This laboratory exercise will reinforce and prove most of the principles of RC oscillators. Then, too, it will illustrate to you the particular symptoms that selected faulty components will cause. And, you will gain valuable experience in the use of multimeters and oscilloscopes as an aid to circuit checking and troubleshooting.

ANSWERS TO B:

1. c
2. emitter, R3, R4.
3. is, is not
4. d
5. A
6. degenerative, regenerative
7. a decrease, no change
8. b

If you missed ANY questions, review the material before you continue.

YOU MAY STUDY ANOTHER RESOURCE OR TAKE THE MODULE SELF-CHECK.

LABORATORY EXERCISE

44-1

SOLID STATE RC OSCILLATORS

OBJECTIVE: Given a trainer, multimeter, and oscilloscope, measure the output amplitude and frequency of an RC oscillator circuit within ± 10 percent accuracy.

NOTE: Upon completion of the Progress Check, have your instructor initial this objective on your check list.

EQUIPMENT:

1. Phase Shift Oscillator Trainer (5016)
2. Oscilloscope (LA-261)
3. Multimeter (AN/PSM-6)
4. Transistor Power Supply (4649)

REFERENCE: Student Text, Volume 6, paragraphs 2-84 thru 2-91.

CAUTION: OBSERVE BOTH PERSONNEL AND EQUIPMENT SAFETY RULES AT ALL TIMES. REMOVE WATCHES AND RINGS.

PROCEDURES: 1. Equipment Preparation

a. Oscilloscope Controls

Oscilloscope Controls	Position
(1) POWER	ON
(2) VOLTS/DIV	"A" 5 (Calibrated) "B" 1 (Calibrated)
(3) MODE	Alternate
(4) POLARITY	Normal, AC
(5) TIME/DIV	.2 millisec
(6) TRIGGER SELECTOR	AUTO, Ext, +
(7) HORIZONTAL POSITION	Adjust for NORMAL sweep
(8) FOCUS and INTENSITY	Adjust for CLEAR presentation

NOTE: Oscilloscope controls can be changed to facilitate work, or to provide more accurate readings.

b. Trainer: Turn R-105 to the fully clockwise position.

c. Interconnections:

(1) Connect Power Supply to Trainer. (Use Jones Plug Cable.)

(2) Ground Oscilloscope to Trainer.

(3) Connect Trigger Input to TP-106.

(4) Connect "A" Channel probe to TP-105.

d. Power Supply

(1) ON/OFF Switch - ON

(2) Adjust for 22 volts. (Use built-in meter.)

2. Trainer Analysis

In order to produce an audio frequency using LC components, the value of inductance at this low frequency would have to be large. As a result the inductive component would have to be physically large. This disadvantage is overcome by generating audio frequencies using an RC oscillator. This trainer is a typical example of an RC oscillator used in generating an audio signal.

3. Activity

a. Measure the amplitude of the signal on the collector of Q-101. Measure the time required for one cycle. Record your measurements in the spaces below.

Amplitude ____________________ Volts pk/pk.

Time for one cycle ____________________ milliseconds.

b. Calculate the frequency ($f = \frac{1}{t}$) of oscillations, and record in the space below.

Frequency ____________________ Hz.

c. Leaving "A Channel" probe in TP-105, use "B Channel" probe to measure the signal amplitude at the following test points, and record results in blanks provided.

TP-101 ____________________ volts PP.

TP-102 ____________________ volts PP.

TP-103 ____________________ volts PP.

d. Underline the correct response to the following statements:

(1) The oscillator is producing a signal in the (audio) (radio) frequency range.

(2) Amplitude of the feedback signal is (increased) (decreased) by each RC section in the feedback path.

(3) From collector to base, the feedback signal is shifted a total of (0) (60) (90) (120) (180) degrees, providing (regenerative) (degenerative) feedback for sustaining oscillations.

e. Leaving "A Channel" probe in TP-105 and "B Channel" probe in TP-103 rotate R-105 completely counterclockwise (NOTE: If your trainer ceases oscillation with R-105 in the completely CCW position, rotate R-105 back in a CW direction until oscillations recur.) Measure the amplitude of the output (TP-105) and feedback (TP-103) signals, and record in the blanks provided.

TP-105 ____________________ volts PP.

TP-103 ____________________ volts PP.

f. Underline the correct response to the statement following:

Rotating R-105 in a CCW direction cause feedback amplitude to (increase) (decrease) and output amplitude to (increase) (decrease).

g. Rotate R-105 in a completely CW direction. Remove "B Channel" probe from TP-103. Leaving "A Channel" probe connected to TP-105, connect a test lead between TP-103 and ground.

Underline the correct response to the following statement:

Amplitude of output oscillations was (increased) (decreased to 0) because the test lead is effectively (opening) (shorting) R-103 and the emitter to base junction.

h. Move the test lead from TP-103 to TP-102. Underline the correct response to the following statement:

The circuit (is) (is not) oscillating because the (regenerative feedback is being shorted to ground) (forward bias has been reduced to zero).

i. Remove the test lead from TP-102. Place the multimeter FUNCTION switch on 1000 Ohms/Volt DC, and the RANGE switch on 1000. Connect the voltmeter between TP-101 and ground. Observe the signal at TP-105. Change the multimeter range switch thru all ranges down to the 10 volt range. Measure the time required for one cycle, and calculate the oscillator frequency. Record your results in the spaces provided.

LABORATORY EXERCISE

Time for one cycle = ______________________ milliseconds.

Frequency = __________________ Hz.

(NOTE: The internal resistance of the voltmeter is being connected in parallel with R-101. When the RANGE switch is changed, the internal resistance of the meter changes, effectively changing the resistance of R-101. As the RANGE switch is changed downward, the internal resistance of the multimeter decreases).

Underline the correct response to the following statement:

As resistance of R-101 effectively was decreased, the time required for one cycle (increased) (decreased) and the frequency (increased) (decreased).

j. Summary: Underline the correct response to the following statements:

(1) The RC oscillator circuit used for this trainer uses (two) (three) RC sections to shift the signal from collector to base a total of (0) (60) (120) (180) degrees, providing regenerative feedback for (only one) (more than one) frequency.

(2) Decreasing the amount of regenerative feedback causes (a decrease) (an increase) (no change) in output amplitude, and (an increase) (a decrease) (no change) in output frequency.

(3) Shorting either of the resistors in the RC phase shift networks causes the oscillator to (oscillate at a lower frequency) (cease oscillating).

(4) Decreasing the resistance of either one of the resistors in the phase shift networks causes the oscillator to (cease oscillating) (oscillate at a higher frequency) (oscillate at a lower frequency).

CONFIRM YOUR RESPONSES ON THE NEXT EVEN NUMBERED PAGE.

NOTES

ANSWERS TO LABORATORY EXERCISE:

3. a) Amplitude 14 volts pk/pk

Time for one cycle .32 milliseconds.

b) Frequency 3,125 Hz.

c) TP-101 4 volts PP.
TP-102 1 volts PP.
TP-103 .1 volts PP.

d) (1) audio
(2) decreased
(3) 180, regenerative

e) TP-105 6.6 volts PP.
TP-103 .06 volts PP.

f) decrease, decrease

g) decreased to 0, shorting

h) is not, the regenerative feedback is being shorted to ground

i) (1) .25 milliseconds.

(2) 4,000 Hertz.

(3) decreased.

(4) increased.

j) (1) three, 180, only one
(2) a decrease, no change
(3) cease oscillating
(4) oscillate at a higher frequency.

If your response to ANY of the statements is wrong, or if ANY of your measurements are more than 10% different from those given, go back and repeat that portion of the Laboratory Exercise. If necessary, review the referenced text for clarification. Your instructor will assist you if needed.

CONSULT YOUR INSTRUCTOR FOR PROGRESS CHECK.

YOU MAY STUDY ANOTHER RESOURCE OR TAKE THE MODULE SELF-CHECK .

SOLID STATE RC OSCILLATORS

For questions 1 and 2, match the schematic diagram (Figure 6 and 7) to the names of oscillators.

__________ 1. RC Phase Shift

__________ 2. Wien Bridge

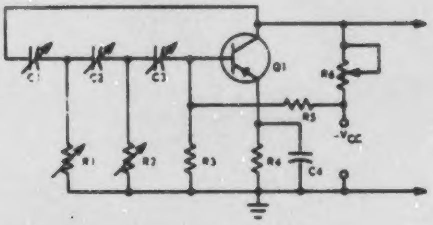

C1
C2
C3
Q1
R6
R5
-Vcc
R1
R2
R3
R4
C4

Figure 6

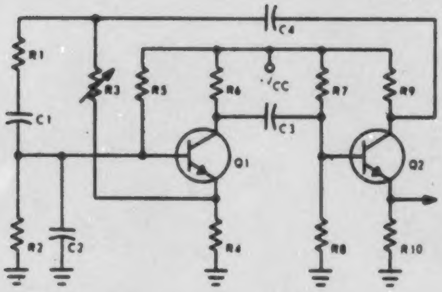

C4
R1
R3
R5
R6
-Vcc
R7
R9
C1
C3
Q1
Q2
R2
C2
R4
R8
R10

Figure 7

For questions 3 thru 6 refer to Figure 6.

3. This oscillator contains (1, 2, 3) phase shift networks with the purpose of shifting the signal between the collector and base of Q1 a total of (0, 60, 120, 180) degrees.

4. The regenerative feedback loop for this oscillator consists of Q1,

__________ a. R6, and R5.

__________ b. R6, power source, and R3.

__________ c. C1, C2, and C3.

__________ d. C1, R1, and R3.

MODULE SELF-CHECK

5. Symptom: Circuit is not oscillating; V_C is high; forward bias has decreased. A possible trouble is

__________ a. C3 open.
__________ b. C3 shorted.
__________ c. C2 open.
__________ d. C2 shorted.

6. Symptom: No output signal; V_C is very low. A possible trouble is

__________ a. Q1 open.
__________ b. Q1 shorted.
__________ c. R4 open.
__________ d. C3 shorted.

For questions 7 thru 10 refer to Figure 7.

7. The purpose of C4 is to couple

__________ a. regenerative feedback only.
__________ b. degenerative feedback only.
__________ c. both regenerative and degenerative feedback.
__________ d. the output signal to the amplifier.

8. The purpose of R3 is to control

__________ a. degenerative feedback amplitude.
__________ b. regenerative feedback amplitude.
__________ c. degenerative and regenerative feedback amplitude.
__________ d. regenerative feedback and bias applied to Q1.

9. Amplitude of regenerative feedback on the base of Q1 is higher (above, at, below) the center of the frequency band.

10. The frequency determining device of this circuit is composed of

__________ a. R6, C3, and R7.
__________ b. R1, C1, R2, and C2.
__________ c. C4, R3, and R4.
__________ d. C3, Q2, C4, and Q1.

CONFIRM YOUR ANSWERS ON THE NEXT EVEN NUMBERED PAGE.

NOTES

MODULE SELF-CHECK

ANSWERS TO MODULE SELF-CHECK

1. Figure 6
2. Figure 7
3. 3, 180
4. c. C1, C2, and C3.
5. b. C3 shorted.
6. b. Q1 shorted.
7. c. both regenerative and degenerative feedback.
8. a. degenerative feedback amplitude.
9. at
10. b. R1, C1, R2, and C2.

HAVE YOU ANSWERED ALL OF THE QUESTIONS CORRECTLY? IF NOT, REVIEW THE MATERIAL OR STUDY ANOTHER RESOURCE UNTIL YOU CAN ANSWER ALL QUESTIONS CORRECTLY. IF YOU HAVE, CONSULT YOUR INSTRUCTOR FOR FURTHER GUIDANCE.

☆ U. S. GOVERNMENT PRINTING OFFICE: 1974-671-158/127

CHANGE 1
KEP-GP-44
1 September 1974
Effective 1 February 1976

Page 1 Objective: a. From a schematic diagram of any one of the following oscillators, select the component(s) that comprise the feedback loop(s), frequency determining device, forward bias network, amplitude adjustment, and the frequency adjustment: Phase Shift; Wien Bridge.

b. Given a trainer and oscilloscope, measure and calculate the phase shift in degrees of each RC network of an RC oscillator within ± 10 percent accuracy.

Page 8 Question 6 Symptoms: V_C is higher than normal (almost equal to V_{CC}) and there is no output. A possible trouble is

______________ a. C3 open.

______________ b. C3 shorted.

______________ c. C4 shorted.

______________ d. C4 open.

Page 9 Question 10 Symptoms: V_C is very close to V_{CC} and there is no output. A possible trouble is

______________ a. C3 open.

______________ b. C4 shorted.

______________ c. R3 open

______________ d. R5 open

Page 13 through 18 Use the following Laboratory Exercise

LABORATORY EXERCISE

44-1

SOLID STATE RC OSCILLATORS

OBJECTIVE: Given a trainer and oscilloscope, measure and calculate the phase shift in degrees of each RC network of an RC oscillator within ± 10 percent accuracy.

EQUIPMENT: 1. Phase Shift Oscillator Trainer

2. Oscilloscope

3. Multimeter

4. Transistor Power Supply

REFERENCE: Student Text, volume 6, paragraphs 2-84 thru 2-91.

CAUTION: **OBSERVE BOTH PERSONNEL AND EQUIPMENT SAFETY RULES AT ALL TIMES. REMOVE WATCHES AND RINGS.**

PROCEDURES:

1. Trainer Analysis.

   a. A schematic diagram of the trainer is shown in figure 44-1.

   b. The purpose of each component is as follows:

      (1) R106 and R105 make up the collector load for Q101.

      (2) R103 and R104 make up the forward bias network for Q101. R103 is also part of the frequency determined network.

      (3) Q101 is the amplifier in the RC oscillator.

      (4) C101, R101, C102, R102, C103, and R103 form both the feedback loop and the frequency determining device.

   c. Each network will shift the feedback signal approximately 60° and the transistor will shift the phase 180°. These shifts will total 360° at only one frequency.

2. Preparation of Equipment

a.

OSCILLOSCOPE CONTROLS	POSITION
(1) Power	ON
(2) CH1 and CH2 Vertical Position	Mid-range
(3) AC/GND/DC, CH1 and CH2	AC
(4) VOLTS/CM, CH1	5 CAL
(5) VOLTS/CM, CH2	20mV CAL
(6) SEPARATE/CH1&CH2	SEPARATE
(7) AC/ACF/DC	AC

(8)	CHOP/ALT	ALT
(9)	TRIG SELECT	CH1 +
	LEVEL	AUTO
(10)	TIME/CM	50μs CAL
(11)	FOCUS and INTENSITY	well defined sweep
(12)	PULL TO INVERT CH2	Push In (Normal)

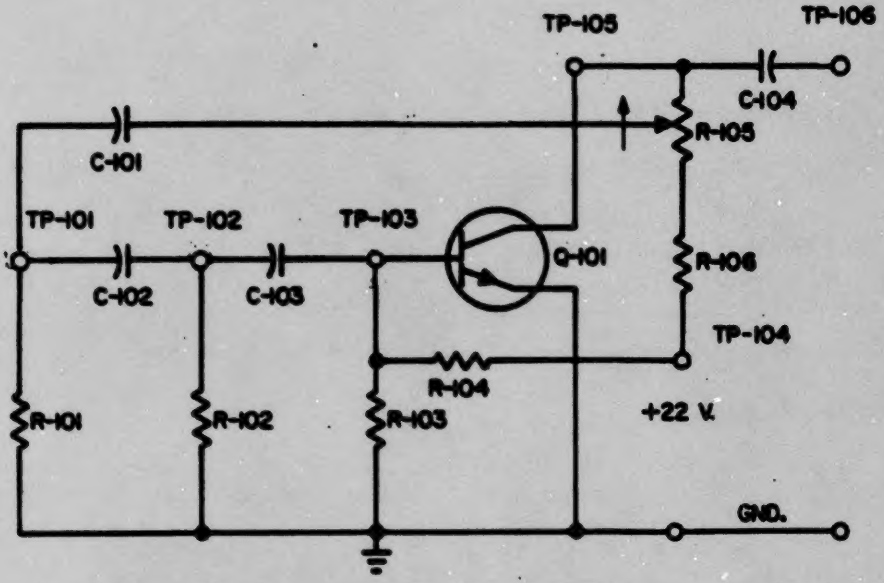

TP-105
TP-106
C-104
R-105
C-101
TP-101
TP-102
TP-103
Q-101
R-106
C-102
C-103
TP-104
R-104
+22 V.
R-101
R-102
R-103
GND.

Figure 44-1. Phase Shift Oscillator

b. TRAINER CONTROL

R105 fully clockwise

c. POWER SUPPLY

(1) Connect trainer to power supply.

(2) Turn power supply on.

(3) Set voltage to 22 volts DC using meter on power supply.

3. Activity.

a. Connect the oscilloscope to trainer

(1) CH1 probe to TP105 and GND.

(2) CH2 probe to TP103 and GND.

b. Observe the waveform (CH2) at TP103 (base of Q101), and if distortion is present adjust R105 counterclockwise until the distortion disappears.

c. Measure and record the output voltage (CH1), time for one cycle, and calculate the output frequency as it appears at TP105. ($f = \frac{1}{t}$)

(1) Collector voltage________________volts Pk-Pk.

(2) Time for one cycle______________milliseconds.

(3) Output frequency____________Herts.

d. Leaving CH1 connected to TP105, measure and record the voltages through the RC phase shift network using CH2.

(1) TP101_________________volts Pk-Pk

(2) TP102_________________volts Pk-Pk

(3) TP103_________________volts Pk-Pk

e. Measure and record the phase shift across each of the RC networks. Use the following procedures to measure phase relationships.

(1) To measure the phase shift across C101 compare the waveshapes at TP105 and TP101. CH1 to TP105 and CH2 to TP101.

(2) Using both channel VOLTS/CM and VARIABLE controls, adjust both waves to the same amplitude and as large as possible on the display.

(3) Set both channel AC/GND/DC controls to GND and position both traces on the horizontal center line of the display.

(4) Return CH1 AC/GND/DC to AC. Using the TIME/CM and VARIABLE controls, set one cycle to cover exactly 8 cm. This is a reference.

NOTE: You now have one cycle (360°) covering 8 cm. Therefore 1 cm is equal to 45°. Each small division (.2cm) is equal to 9°.

(5) Place CH2 AC/GND/DC switch to AC, measure the time difference between the two waves and convert to degrees.

(6) Record phase shift across C101.
______________degrees.

(7) To check the phase shift across C102, compare waveshapes at TP101 and TP102 with CH1 at TP101 and CH2 at TP102.

(8) Using steps 2 thru 5 in procedure 3e, measure and record the phase shift across C102.
________________degrees.

(9) Move CH1 to TP102 and CH2 to TP103, measure and record the phase shift across C103.
_______________degrees.

f. The calculated total phase shift across the RC networks is _______degrees.

g. To measure total phase shift:

(1) Connect CH1 to TP105 and CH2 to TP103.

(2) Follow steps 3e(2) thru 3e(5) to measure and record the total phase shift.
______________degrees.

4. Summary:

a. Consolidate the readings taken in the lab project for the following:

(1) Output frequency_______________Hertz 3c(3).

(2) Transistor output voltage_______volts 3c(1).

(3) Phase shift C101_________degrees 3e(6).

(4) Voltage at TP101________volts 3d(1).

(5) Phase Shift C102_________degrees 3e(8).

(6) Voltage at TP102_________volts 3d(2).

(7) Phase shift C103_________degrees 3e(9).

(8) Transistor input voltage________volts 3d(3).

b. The phase shift across each RC network is approximately___________ degrees.

c. The total phase shift across the three RC networks is approximately __________degrees.

CONFIRM YOUR ANSWERS.

ANSWERS TO LABORATORY 44-1

3. c. (1) 8 to 12 volts.

(2) .25 to .4 milliseconds.

(3) 2500 to 4000 Hertz.

d. (1) 2 to 3 volts.

(2) .5 to 1.5 volts.

(3) 20 to 60 millivolts.

e. (6) 45 to 60 degrees.

(8) 45 to 60 degrees.

(9) 60 to 89 degrees.

f. 185 to 195 degrees.

g. (2) 185 to 195 degrees.

4. a. (1) 2500 to 4000 Hertz.

(2) 8 to 12 volts.

(3) 45 to 60 degrees.

(4) 2 to 3 volts.

(5) 45 to 60 degrees.

(6) .5 to 1.5 volts.

(7) 60 to 89 degrees.

(8) 20 to 60 millivolts.

b. 60 degrees.

c. 180 degrees.

If your response to ANY of the statements is wrong, or if ANY of your measurements are more than 10% different from those given go back and repeat that portion of the Laboratory Exercise. If necessary, review the referenced text for clarification. Your instructor will assist you if needed.

CONSULT YOUR INSTRUCTOR FOR PROGRESS CHECK.

YOU MAY STUDY ANOTHER RESOURCE OR TAKE THE MODULE SELF-CHECK.

PREPARE THE MAN

ATC GP 3AQR3X020-X
Prepared by Keesler TTC
KEP-GP-45

Technical Training

ELECTRONIC PRINCIPLES (MODULAR SELF-PACED)

MODULE 45

SOLID STATE FREQUENCY MULTIPLIERS

1 October 1975

7-10

AIR TRAINING COMMAND

Designed For ATC Course Use

ATC Keesler 6-1981

DO NOT USE ON THE JOB

Radar Principles Branch
Keesler Air Force Base, Mississippi

ATC GP 3AQR3X020-X
KEP-GP-45
1 October 1975

ELECTRONIC PRINCIPLES (MODULAR SELF-PACED)

MODULE 45

SOLID STATE FREQUENCY MULTIPLIERS

This Guidance Package is designed to guide you through this module of the Electronic Principles Course. This Guidance Package contains specific information, including references to other resources you may study, enabling you to satisfy the learning objectives.

CONTENTS

TITLE	PAGE
Overview	1
List of Resources	1
Adjunct Guide	1
Module Self-Check	2
Answers	4

OVERVIEW

1. SCOPE: Quite often it is impractical for a particular oscillator to produce a frequency high enough to meet the requirements. And, it is quite common in such cases to produce the higher frequency by having the oscillator produce a relatively low frequency, and then multiplying the oscillator's output as much as required to reach the needed frequency. This module will discuss how this multiplication is accomplished.

2. OBJECTIVE: Upon completion of this module you should be able to satisfy the following objective:

Given a schematic diagram of a frequency multiplier, (with component values given) and the input frequency to the frequency multiplier, determine its output frequency and the factor by which its input frequency will be multiplied in the output.

LIST OF RESOURCES

To satisfy the objectives of this module, you may choose, according to your training, experience, and preferences, any or all of the following:

READING MATERIALS:

Digest
Adjunct Guide with Student Text VI

AT THIS POINT, IF YOU FEEL THAT THROUGH PREVIOUS EXPERIENCE OR TRAINING YOU ARE FAMILIAR WITH THIS SUBJECT, YOU MAY TAKE THE MODULE SELF-CHECK. IF NOT, SELECT ONE OF THE RESOURCES AND BEGIN STUDY.

CONSULT YOUR INSTRUCTOR IF YOU NEED HELP.

Supersedes KEP-GP-45, dated 1 June 1974. Supplies on hand will be used.

ADJUNCT GUIDE

INSTRUCTIONS:

Study the referenced materials as directed.

Return to this guide and answer the questions.

Check your answers against the answers at the back of this Guidance Package.

Contact your instructor if you experience any difficulty.

Begin the program.

The use of frequency multipliers is common in electronics systems. Their use is especially common in equipment requiring a very stable, extra high frequency.

For instance, you should recall that a quartz crystal oscillator affords the best frequency stability. However, the highest frequency that a crystal oscillator, such as the Butler you previously studied, can operate is determined by physical limitations. The higher the frequency desired, the thinner the crystal must be ground. Eventually, a point is reached where the quartz crystal wafer is so thin that it would shatter if caused to vibrate.

The advantage of exceptionally good frequency stability of a crystal oscillator is maintained, and the disadvantage of a shattered crystal is overcome, by using a lower frequency crystal and then multiplying its output as many times as required to produce the desired frequency.

A. Turn to Student Text, Volume VI, and study paragraphs 2-105 through 2-112. Return to this page and respond to the following statements/questions.

1. A frequency multiplier will most likely operate Class (A) (C) in order to (produce) (prevent) harmonics of the fundamental frequency.

2. A Butler oscillator is producing a frequency of 430 kHz. It is followed by a doubler, a tripler, and a quadrupler. The output frequency of the quadrupler is:

   a. 3870 kHz

   b. 10.32 MHz

   c. 3.87 MHz

   d. 1032 kHz

3. Given the figure 45-1 schematic diagram with tank circuit component values, the resonant frequency of the tank circuit is __________ kHz. (Use the formula: $f_o = \frac{.159}{\sqrt{LC}}$ and carry answer to 4 decimal places.)

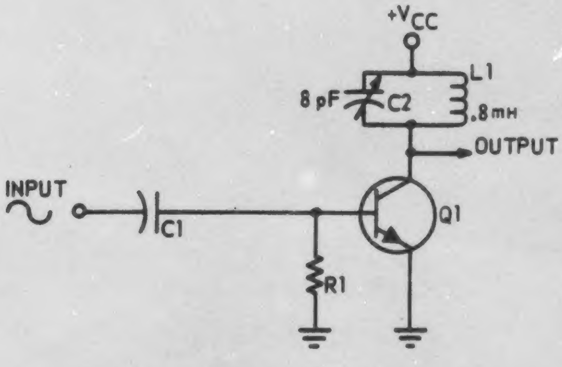


Figure 45-1

4. With an input frequency of 660 kHz, the frequency multiplier will act as a (doubler) (tripler) (quadrupler).

5. A frequency multiplier serves as a (rectifier) (buffer).

6. The frequency multiplier (does) (does not) require neutralization.

CONFIRM YOUR ANSWERS AT THE BACK OF THIS GUIDANCE PACKAGE.

YOU MAY STUDY ANOTHER RESOURCE OR TAKE THE MODULE SELF-CHECK.

MODULE SELF-CHECK

QUESTIONS:

All questions refer to the circuit in figure 45-2.

1. This circuit is correctly identified as a

______________________ ________________.

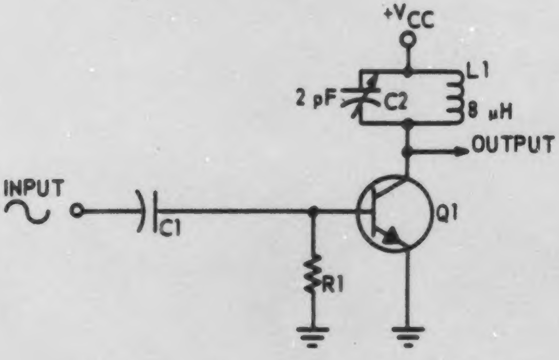
2. This circuit is normally operated class (A) (C) in order to (develop) (prevent) harmonics.

3. With the given values of tank circuit capacitance and inductance, and the input frequency of 10 megahertz, this circuit would act as a frequency (doubler) (tripler) (quadrupler).

4. In addition to multiplying frequency, this circuit will act as a (voltage doubler) (buffer).

5. If the input frequency to this circuit is changed to 20 megahertz, the output frequency will (increase) (decrease) (remain the same); and the circuit will be a (doubler) (tripler) (quadrupler).

CONFIRM YOUR ANSWERS AT THE BACK OF THIS GUIDANCE PACKAGE.



REP4-1434

Figure 45-2

ANSWERS TO A - ADJUNCT GUIDE

1. C, produce
2. b
3. 1980 kHz
4. tripler
5. buffer
6. does not

If you missed ANY questions, review the material before you continue.

ANSWERS TO MODULE SELF-CHECK

1. frequency multiplier
2. C, develop
3. quadrupler
4. buffer
5. remain the same, doubler

HAVE YOU ANSWERED ALL OF THE QUESTIONS CORRECTLY? IF NOT REVIEW THE MATERIAL OR STUDY ANOTHER RESOURCE UNTIL YOU CAN ANSWER ALL QUESTIONS CORRECTLY. IF YOU HAVE, CONSULT YOUR INSTRUCTOR FOR FURTHER INSTRUCTIONS.

ATC GP 3AQR3X020-X
Prepared by Keesler TTC
KEP-GP-46

Technical Training

Electronic Principles (Modular Self-Paced)

Module 46

SOLID STATE PULSED AND BLOCKING OSCILLATORS

November 1975

AIR TRAINING COMMAND

7-10

Designed For ATC Course Use

ATC Keesler 6-2564

DO NOT USE ON THE JOB

Radar Principles Branch
Keesler Air Force Base, Mississippi

ATC GP 3AQR3X020-X
KEP-GP-46
November 1975

ELECTRONIC PRINCIPLES (MODULAR SELF-PACED)

MODULE 46

SOLID STATE PULSED AND BLOCKING OSCILLATORS

This Guidance Package is designed to guide you through this module of the Electronic Principles Course. This Guidance Package contains specific information, including references to other resources you may study, which will enable you to satisfy the learning objectives.

CONTENTS

Title	Page
Overview	1
List of Resources	1
Adjunct Guide	1
Module Self-Check	5
Answers	7

OVERVIEW

1. SCOPE: A pulsed oscillator is normally a sine wave oscillator that is gated (turned on and off) to produce an output for a specified period, and is then turned off for a specified period. A blocking oscillator, on the other hand, produces a constant output of narrow pulses used for timing purposes. In this module you will learn how the output signal is produced from each of these circuits, and specific components that affect the output and feedback arrangements.

2. OBJECTIVES: Upon completion of this module you should be able to satisfy the following objectives.

a. Given a collector loaded pulsed oscillator schematic diagram with an input gate and a group of waveforms, select the output.

b. From a schematic diagram of a blocking oscillator, select the component(s) that primarily determine output signal pulse width; that determine output signal pulse recurrence time; that determine transistor cutoff time; that provide forward bias for the transistor.

c. Given the schematic diagram of a blocking oscillator and descriptive statements and waveforms, match the waveform to the statement.

d. Given the schematic diagram of a synchronized blocking oscillator and a group of waveforms, select the ideal waveform that would be present in the feedback loop and in the output circuit.

LIST OF RESOURCES

To satisfy the objectives of this module you may choose, according to your training, experience, and preferences, any or all of the following.

READING MATERIALS:

Digest
Adjunct Guide with Student Text VI

Supersedes KEP-GP-46, dated 1 August, 1974. Supplies on hand will be used.

AT THIS POINT, IF YOU FEEL THAT THROUGH PREVIOUS EXPERIENCE OR TRAINING YOU ARE FAMILIAR WITH THIS SUBJECT, YOU MAY TAKE THE MODULE SELF-CHECK.

CONSULT YOUR INSTRUCTOR IF YOU NEED HELP.

ADJUNCT GUIDE

The circuits you will study in this module include the pulsed oscillator and the blocking oscillator. These circuits are used in radar and communications equipments.

INSTRUCTIONS:

Study the referenced materials as directed.

Return to this guide and answer the questions.

Check your answers against the answers at the back of this Guidance Package.

Contact your instructor if you experience any difficulty.

Begin the program.

A. Turn to Student Text, Volume VI, and study paragraphs 3-1 through 3-20. Return to this page and answer the following statements/questions.

1. In each of the three different pulsed oscillators discussed in the Student Text, the transistor to which the input gate is applied acts as a (switch) (amplifier), and the transistor must be (cut off) (saturated) in order for the circuit to produce a sine wave output.

2. The rate of damping of the sine wave output from the collector-loaded and emitter-loaded pulsed oscillator without regeneration is controlled by the:

___a. Amplification factor of the transistor.

___b. Q of the tank circuit.

___c. Amplitude of the feedback.

___d. Amplitude of the input gate.

3. Sine waves would be generated at the emitter of Q1 (figure 46-1) during which time period of the input gate?

___a. T0 to T2.

___b. T1 to T2.

___c. T0 to T1 and T2 to T3.

___d. T0 to T2 and T1 to T3.

4. Frequency of the sine wave appearing at the emitter of Q1 (figure 46-1) is determined by the (input gate width) (value of L1 and C2).

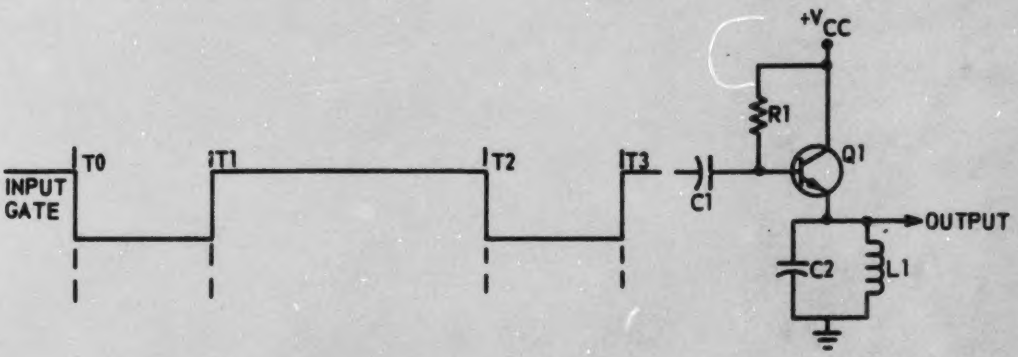
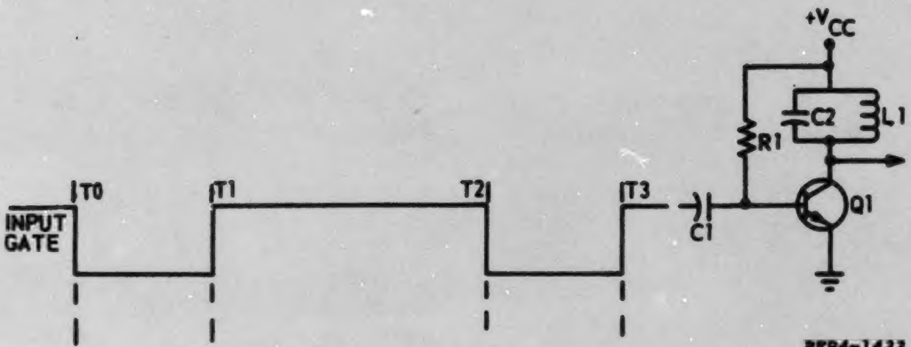


Figure 46-1. Pulsed Oscillator


+VCC
C2
L1
R1
Q1
C1
T0
T1
T2
T3
INPUT GATE

REP4-1433

Figure 46-2. Schematic Diagram

Refer to figure 46-2 for questions 5 and 6.

5. The schematic represents a (collector) (emitter)-loaded pulse oscillator (with) (without) regeneration.

6. The circuit will produce a (sine) (square) wave output from T___ to T___ and T___ to T___ of the input gate.

For questions 7 through 9, refer to figure 46-3.

7. A (positive) (negative) gate on the base of Q1 causes it to (cut off) (saturate), producing a sine wave output.

8. The frequency of the sine wave on the collector of Q3 is determined by the:

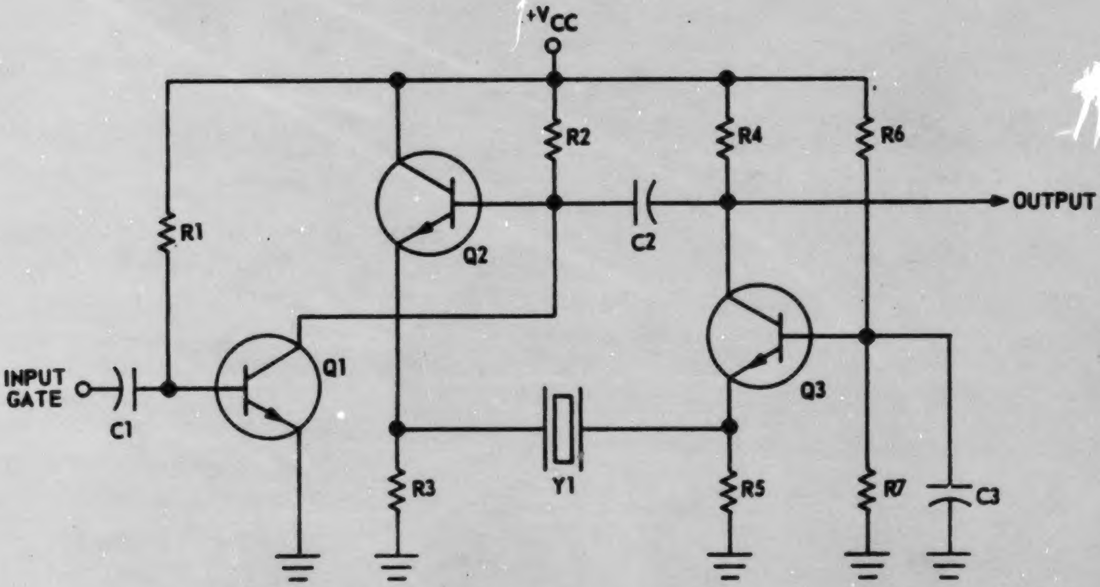
___a. Width of the negative gate on the base of Q1.

___b. Width of the positive gate on the base of Q1.

___c. Circuit RC time constants.

___d. Resonant frequency of Y1.

9. Before an input gate is applied to Q1, Q2 is held at (cutoff) (saturation) by the (low) (high) voltage on the collector of Q1.


+VCC
R2
R4
R6
R1
Q2
C2
OUTPUT
Q1
Q3
INPUT GATE
C1
Y1
R3
R5
R7
C3

REP4-796

Figure 46-3. Crystal Controlled Pulsed Oscillator

NOTES

CONFIRM YOUR ANSWERS.

B. Turn to Student Text, Volume VI, and study paragraphs 4-1 through 4-20. Return to this page and respond to the following statements/questions.

1. A timing pulse should have (fast) (slow) rise time, (flat) (sloping) top, (fast) (slow) fall time, and accurately controlled frequency.

2. The component or components that primarily control the width of the output pulse from a blocking oscillator is/are the:

__a. Resistors and capacitors.

__b. Feedback transformer.

__c. LC tank circuit values.

__d. Input trigger frequency.

3. In a series RL circuit, maximum voltage is dropped across the (resistor) (inductor) at the instant power is applied.

CONFIRM YOUR ANSWERS.

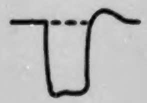
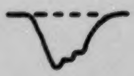
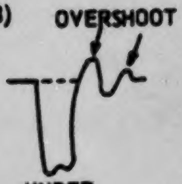
C. Turn to Student Text, Volume VI, and study paragraphs 4-21 through 4-29. Return to this page and answer the following statements/questions.

For questions 1 through 6, refer to figure 46-4.

1. Draw the base waveshape:

```
 T0 T1                       T2  T3
 ,  ,                        ,   ,
0V- - - - - - - - - - - - - - - - - - - - - - - -
```

2. Match the statements in column A to the waveshapes in column B.

A	B
a. Resistance of R2 too high ________	(1)  CRITICAL DAMPING
b. Resistance of R2 correct ________	(2)  OVER DAMPING
c. Resistance of R2 too low ________	(3)  UNDER DAMPING

3. The time from T0 to T2 is controlled by:

__a. R1 and C1 only.

__b. L1 and L2 only.

__c. L1, L2, and R2.

__d. L1, L2, R1, and C1.

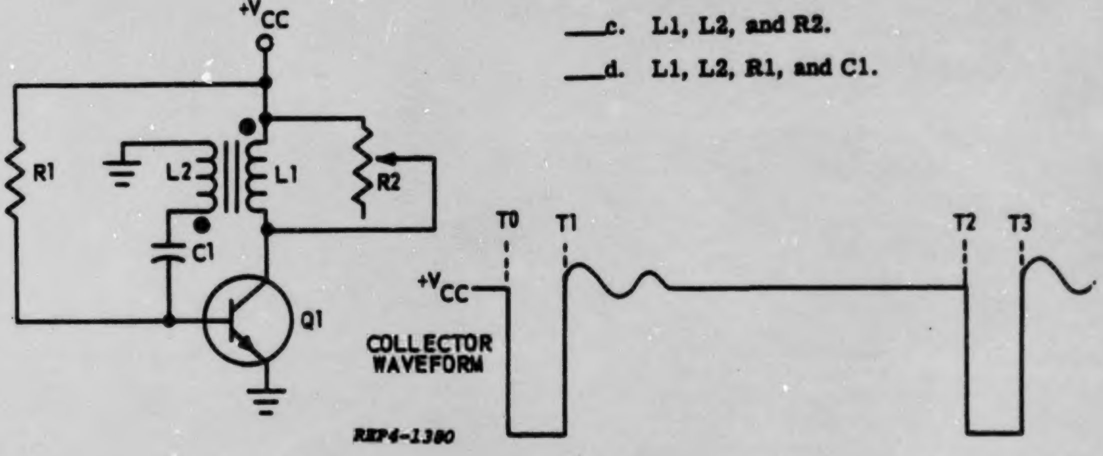


Figure 46-4. Blocking Oscillator

4. Cutoff time of transistor Q1 is controlled by:

___a. R1 and C1 only.

___b. L1 and L2 only.

___c. L1, L2, and R2.

___d. L1, L2, R1, and C1.

5. The time from T0 to T1 is primarily controlled by:

___a. R1 and C1.

___b. L1 and L2.

___c. L1, L2, and R2.

___d. L1, L2, R1, and C1.

6. From T1 to T2, Q1 is (cut off) (saturated), and C1 is (charging) (discharging).

Refer to figure 46-5 for questions 7 through 11.

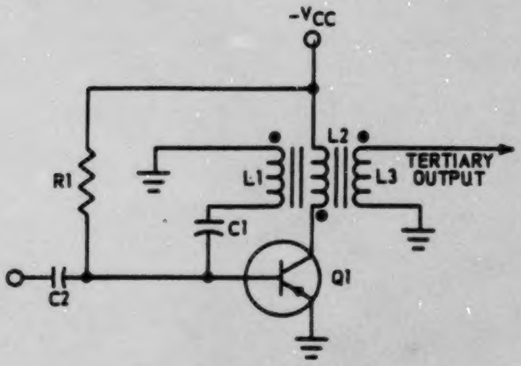


Figure 46-5. Blocking Oscillator

7. Match the statements in column A with the waveshapes in column B.

Column A

a. Signal on the base of Q1 ___________

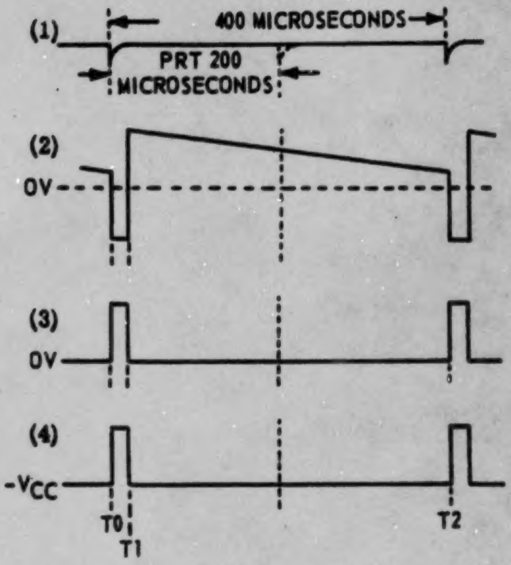
b. Controls PRT ___________

c. Output signal ___________

d. Controls PRF ___________

e. Collector signal ___________

Column B



8. With a trigger input every 200 microseconds (as shown in question 7(1), an output pulse is developed for every (one) (two) input trigger(s).

9. Use the time references of question 7, column B, and list the things that directly affect the following intervals:

a. T0 to T1. ___________

b. T1 to T2. ___________

c. T0 to T2. ___________

10. If C2 became open, which one of the following statements would be true?

___a. The blocking oscillator would not produce an output signal.

___b. The output signal frequency would increase slightly.

2c.

___c. The output signal frequency would decrease slightly.

___d. The output PRT would decrease slightly.

11. Symptoms: V_C is very nearly equal to V_{CC}, and there is no output. A possible trouble is:

___a. R1 open.

___b. C2 open.

___c. Q1 shorted.

___d. L1 open.

CONFIRM YOUR ANSWERS.

YOU MAY STUDY ANOTHER RESOURCE OR TAKE THE MODULE SELF-CHECK.

MODULE SELF-CHECK

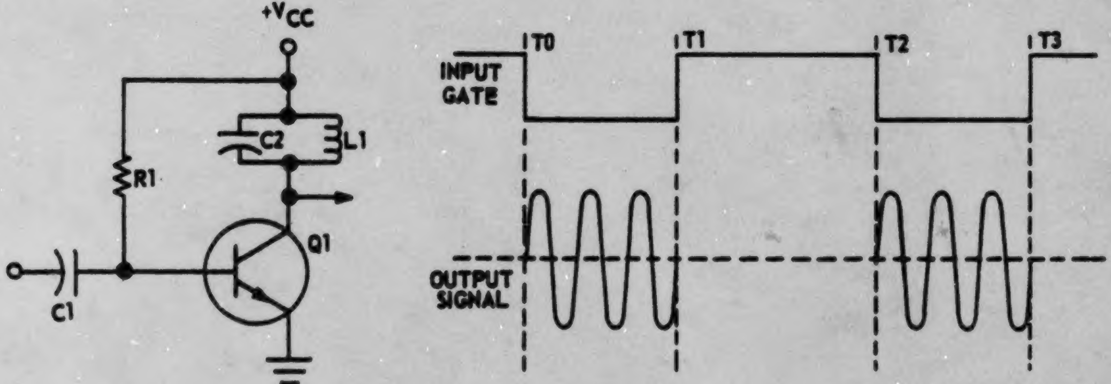
For questions 1 through 3, refer to figure 46-6.

1. The circuit is a (collector) (emitter) -loaded (pulsed) (blocking) oscillator.

2. The sine wave output frequency of this circuit is determined by the (input gate width) (tank circuit values).

3. The length of time this circuit is allowed to oscillate is determined by the (input gate width) (tank circuit values).

For questions 4 through 10, refer to figure 46-7.



REP4-795

Figure 46-6. Circuit Diagram

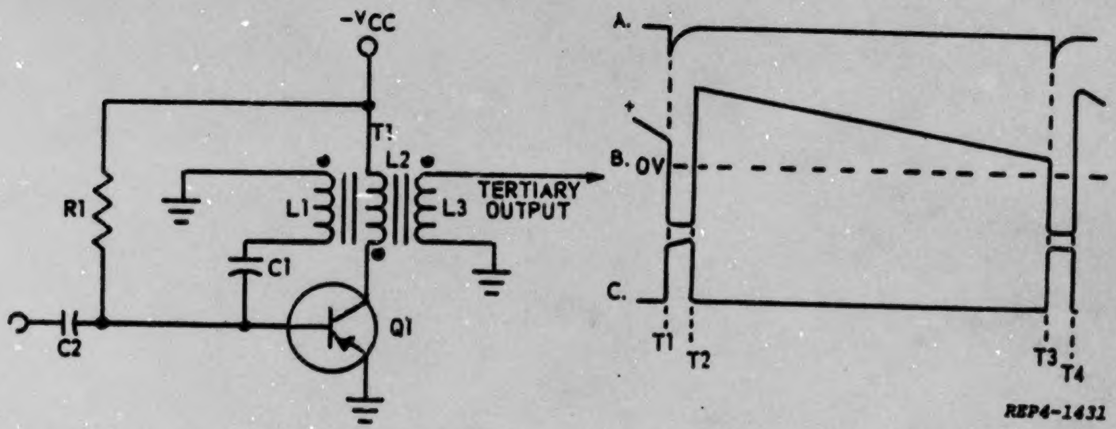

-VCC
T1
R1
L1
L2
L3
C1
C2
Q1
TERTIARY OUTPUT
A.
+
B.
OV
C.
T1
T2
T3
T4
REP4-1431

Figure 46-7. Circuit Diagram

4. This circuit is a (free running) (synchronized) blocking oscillator.

5. Pulse width of the output from this circuit is primarily determined by (trigger frequency) (values of C1 and R1) (T1).

6. Forward bias for this circuit is provided by the current flowing through (R1) (L2) and the (base/collector) (base/emitter) junction.

7. Identify each of the waveforms:

a. Output ______________________

b. Trigger ______________________

c. Feedback ______________________

8. Pulse recurrence time (PRT) is from T___ to T___ or T___ to T___.

9. The time T1 to T2 represents (pulse width) (PRT) (rest time).

10. The time T2 to T3 represents (pulse width) (PRT) (rest time).

CONFIRM YOUR ANSWERS.

ANSWERS TO A:

1. switch, cut off
2. b
3. c
4. Value of L1 and C2
5. collector, without
6. Sine, T0 to T1 and T2 to T3
7. negative, cut off
8. d
9. cutoff, low

If you missed ANY questions, review the material before you continue.

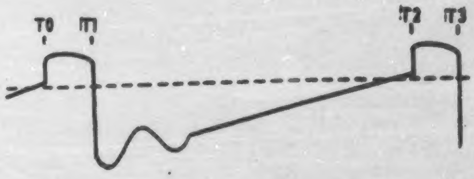
ANSWERS TO B:

1. fast, flat, fast
2. b
3. inductor

If you missed ANY questions, review the material before you continue.

ANSWERS TO C:

1.



2. a. (3)
   b. (1)
   c. (2)
3. d
4. a
5. b
6. cut off, discharging
7. a. (2)
   b. (1)
   c. (3)
   d. (1)
   e. (4)
8. two
9. a. L1 and L2
   b. C1 and R1
   c. Trigger PRT
10. c
11. a

If you missed ANY questions, review the material before you continue.

ANSWERS TO MODULE SELF-CHECK:

1. collector, pulsed
2. tank circuit values
3. input gate width

4. synchronized

5. T1

6. R1, emitter base

7. a. C
   b. A
   c. B

8. T1 to T3 or T2 to T4

9. pulse width

10. rest time

HAVE YOU ANSWERED ALL OF THE QUESTIONS CORRECTLY? IF NOT, REVIEW THE MATERIAL OR STUDY ANOTHER RESOURCE UNTIL YOU CAN ANSWER ALL QUESTIONS CORRECTLY. IF YOU HAVE, CONSULT YOUR INSTRUCTOR FOR FURTHER GUIDANCE.

PREPARE THE MAN

ATC GP 3AQR3X020-X
Prepared by Keesler TTC
KEP-GP-47

Technical Training

ELECTRONIC PRINCIPLES (MODULAR SELF-PACED)

MODULE 47

SOLID STATE MULTIVIBRATORS

1 September 1974

AIR TRAINING COMMAND

7-10

Designed For ATC Course Use

DO NOT USE ON THE JOB

1.
213

Basic and Applied Electronics Department
Keesler Air Force Base, Mississippi

ATC GP 3AQR3X020-X
KEP-GP-47
1 November 1974

ELECTRONIC PRINCIPLES
MODULE 47

This Guidance Package is designed to guide you through this module of the Electronic Principles Course. This Guidance Package contains specific information, including references to other resources you may study, enabling you to satisfy the learning objectives.

CONTENT

TITLE	PAGE
Overview	1
List of Resources	2
Digest	3
Adjunct Guide	9
Laboratory Exercise	23
Module Self-Check	33
Critique	39

Supersedes KEP-GP-47, 1 June 1974, which will be used until the stock is exhausted.

Errata for KEP-GP-47, Dated 1 June and 1 Sept 1974 1 April 1975

PAGE	PARAGRAPH	LINE	CORRECTION
2			Add: AUDIO VISUAL MATERIALS: TV Lesson 30-811, Monostable Multivibrators (40 min)
3	2	3	Correct the spelling of "tirgger" to "trigger".
4	2	2	Space between "The" and "monostable".
4	2	3	After "Q2", delete "And" and capitalize "t" in "the".
*4	3	6	Change the first "R2" to "R3".
4	3	7	Delete the comma after "Q2".
4	Fig 3A		Draw capacitors C3 in parallel with R2 and C4 in parallel with R6.
*6	3rd Symptom		After V_CQ2, delete "equals zero volts" and substitute the word "and".
8	2	2	In the sentence beginnning with "This negative ....", delete the word "negative" and after the word "change", insert "in a positive direction".
8	3	2&3	Delete the sentences beginning with "The collector voltage ......".
*8	8	1	Delete "R6 open".
9	1	3	Add "a" between "than" and "sine".
9	2	5	Change "charactoristics" to "characteristics".
*10	Ques. 1e		Change "PPS" to "kHz".
10	Ques. 2	2	Change both time values to "5" microseconds.
10	Ques. 2		In the schematic, label the capacitor "E_C" and label the resistor "E_R".
11,12,15 thru 18,33, and 34			Substitute the new pages, attached to this errata, for those in your text.

PAGE	PARAGRAPH	LINE	CORRECTION
13	Quest. 5	2	Correct spelling of "incrased" to "increased".
14	Ques. 12c		Change "wuld" to "would".
19	Ques. 9d		Delete "a" in "wouldabe".
22	Answer 4		Delete
23			Delete all of objective #1.
23			Re-number objective 2 to number 1.
23	Procedure 1b3		Change "Jones" to "Bendix".
26	Ques. g(1)		Space between "The" and "trigger".
27		13	Correct the spelling of "decrased" to "decreased".
29	t (9)	15	Place a parenthesis mark between "to" and "o volts , V_{CC}).
*32	t 2.	16	Change "R4" to "R5".
32	Last statement		Change to read "CONSULT YOUR INSTRUCTOR FOR PROGRESS CHECK . . . .".
36	Ques. 16		Change to read "Symptom: V_CQ1 and Q2 = V_{CC}.
37	Figure 16		Label the bottom of R7 "+V_{EE}" and bottom of R2 "+V_{BB}".
37	Ques. 24c		Change "C1" to "R2".

NOTE: The asterisk (*) identifies those additional changes required in the text dated 1 June 1974.

3. Given the RC circuit with square wave input and the associated output waveforms (a through f) in Figure 6, label the output waveshapes as being taken across the resistor (E_R) or the capacitor (E_C).

a.

b.

c.

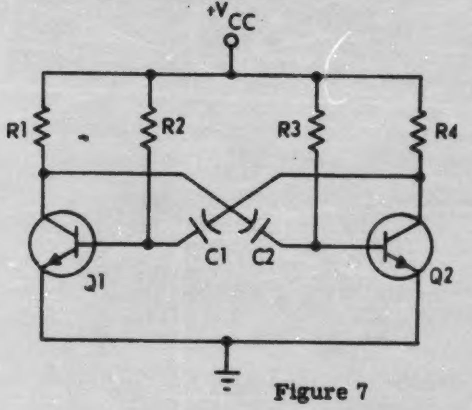
d.

e.

f.

CONFIRM YOUR ANSWERS ON THE NEXT EVEN NUMBERED PAGE.

B. Turn to Student Text, Volume VI, and study paragraphs 5-25 through 5-38. Return to this page and answer the following statements/questions.



REP4-1860

Figure 7

1. Figure 7 is the schematic diagram of a/an ______________________ multivibrator.

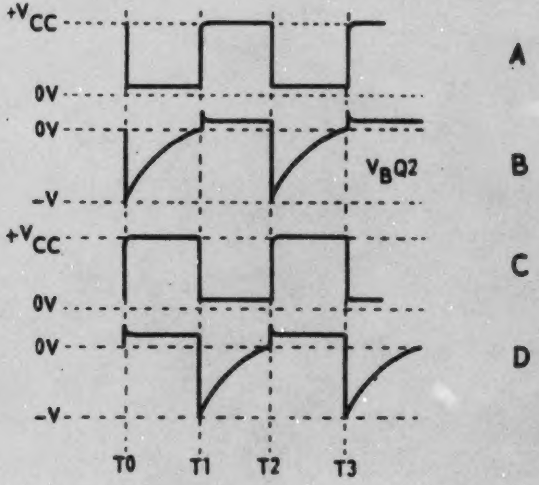
ANSWERS TO A:

1. a. Pulse width = 9.6 microseconds.
   b. Rise Time = 1 microsecond.
   c. Fall time = 1 microsecond.
   d. PRT = 20 microseconds.
   e. PRF = 50 kHz.

2. square, rectangular, no change, no change

3. a. ER
   b. EC
   c. ER
   d. EC
   e. ER
   f. EC

If you mised ANY questions, review the material before you continue.



REP4-1858

Chart 2

C. Turn to Student Text, Volume VI, and study paragraphs 5-40 through 5-48. Return to this page and answer the following statements/questions.

For questions 1 through 6, refer to Figure 9 and Chart 3 as necessary.

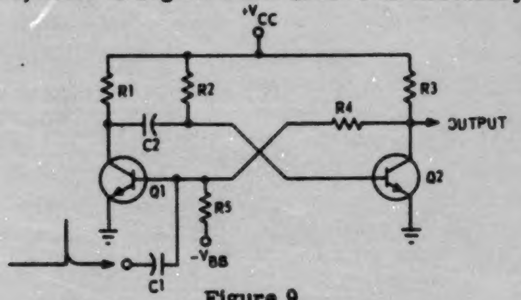


Figure 9

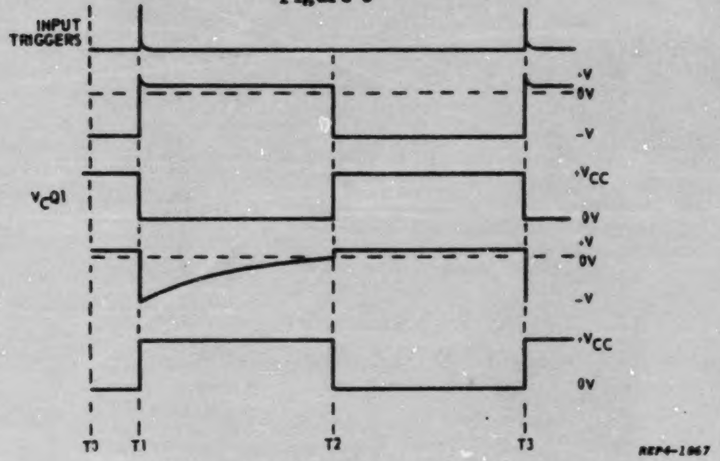


Chart 3

1. Figure 9 is the schematic diagram of a ______________________________;

before triggers are applied, Q ____ is saturated and Q ____ is cutoff.

2. Given Chart 3 as the waveshapes for the Figure 9 circuit, with waveshape "B" labeled as VCQ1, label the remaining waveshapes.

A. ______________________

C. ______________________

D. ______________________

3. An open R ____ would remove forward bias from Q2.

4. Output PRT of the Figure 9 circuit is controlled by the (input trigger PRT) (value of C2 and R2), and output pulse width is controlled by the (input trigger PRT) (value of C2 and R2).

ANSWERS TO B:

1. astable
2. A. VCQ1

   C. VCQ2

   D. VBQ1
3. C1 and R2
4. A. R2

   B. R3

   C. C1

   D. C2
5. a
6. b
7. d
8. Increasing, decrease
9. triggered astable, input trigger frequency
10. higher
11. RC time constants
12. c

If you missed ANY questions, review the material before you continue.

5. Refer to waveform "D" of Chart 3. The time from T1 to T2 could be increased by

_______ a. increasing the value of R2.

_______ b. increasing the trigger PRT.

_______ c. decreasing the value of R2.

_______ d. decreasing the trigger PRT.

6. If C1 (figure 9) became open, which of the following conditions would exist?

_______ a. VCQ2 would remain high and VCQ1 would remain low.

_______ b. VCQ1 would remain high and VCQ2 would remain low.

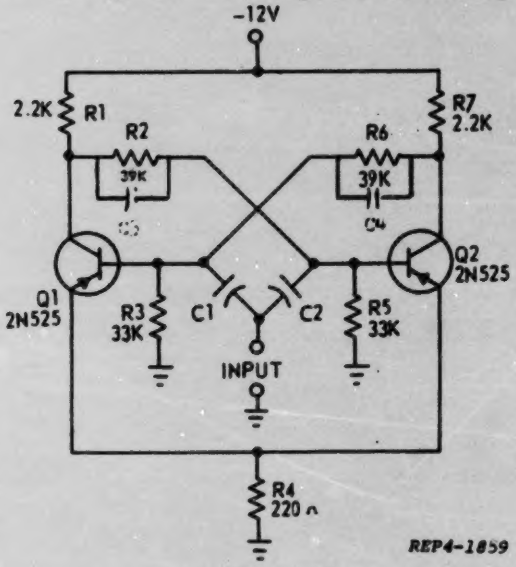
_______ c. The circuit would continue to function, but at a slightly lower frequency.

_______ d. The circuit would continue to function, but at a slightly higher frequency.

CONFIRM YOUR ANSWERS ON THE NEXT EVEN NUMBERED PAGE.

D. Turn to Student Text, Volume VI, and study paragraphs 5-49 through 5-59. Return to this page and answer the following statements/questions.

For questions 1 through 13, refer to Figure 10 and Chart 4 as necessary.



REP4-1859

Figure 10

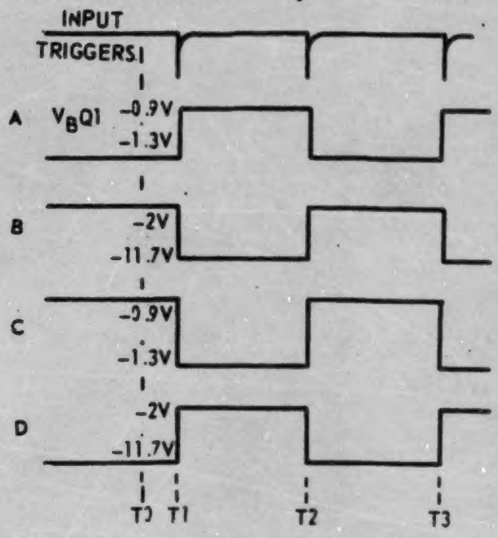


Chart 4

REP4-1865

1. The Figure 10 schematic diagram is correctly identified as a/an ____________________

____________________ multivibrator.

2. Given Chart 4 as the waveshapes for the Figure 10 circuit with waveshape "A" labeled as VBQ1, label the remaining waveshapes.

B. ____________________

C. ____________________

D. ____________________

ANSWERS TO C:

1. Monostable Multivibrator; Q2, Q1

2. A. VBQ1

   C. VBQ2

   D. VCQ2

3. R2

4. input trigger PRT, value of C2 and R2

5. a

6. b

If you missed ANY questions, review the material before you continue.

3. The output PRF of this circuit is controlled by the (input trigger PRF) (RC time constants), and the output pulse width is controlled by the (input trigger PRT) (RC time constants).

4. Complete the following equations:

   a. IR7 = IC Q2 + IR ______

   b. IR4 = (IR1 - IR5) + (IR7 - ______)

   c. V_{CC} = ER1 + ER2 + ER ______

5. Given: The PRT of the input trigger to the Figure 10 circuit is 500 microseconds. The PRF of the output is ____________________ kHz.

6. Which of the following is the path through which forward bias CURRENT for Q2 will flow?

   ______ a. -V_{CC}, R7, collector, emitter, R4, ground.

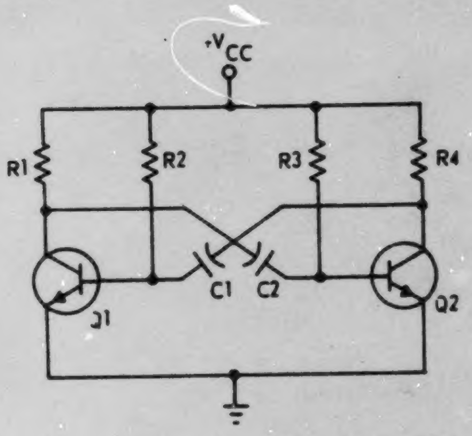
   ______ b. -V_{CC}, R7, R6, R3, ground.

   ______ c. -V_{CC}, R1, R2, R5, ground.

   ______ d. -V_{CC}, R1, R2, base, emitter, R4, ground.

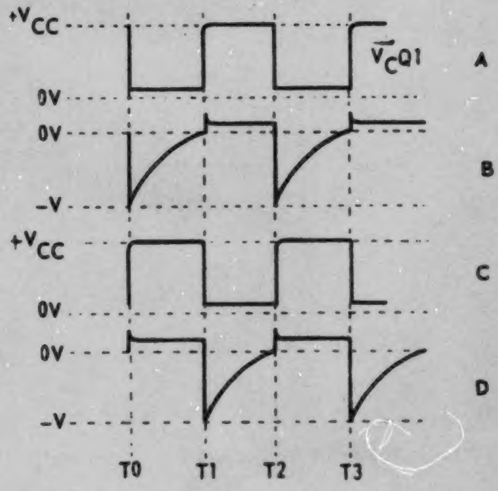
SOLID STATE MULTIVIBRATORS

Questions 1 thru 4, refer to Figure 12 and Chart 5.



REP4-1860

Figure 12



REP4-1858

Chart 9

1. The circuit in Figure 12 is correctly identified as a (triggered, free-running) (astable, monostable, bistable) multivibrator.

2. Given: The waveform labeled "A" on Chart 9 is the signal from the collector of Q2. Match the remaining waveforms to the proper element of the Figure 12 transistors.

Collector Q1 ____________________

Base Q1 ____________________

Base Q2 ____________________

3. Increasing the value of R2 or C1 would cause (Q1, Q2) to be cutoff longer, and (Q1, Q2) to be saturated longer.

4. Given: V_C Q1 and V_C Q2 are very low, and they remain at the same value. A possible trouble is

______ a. R2 open.

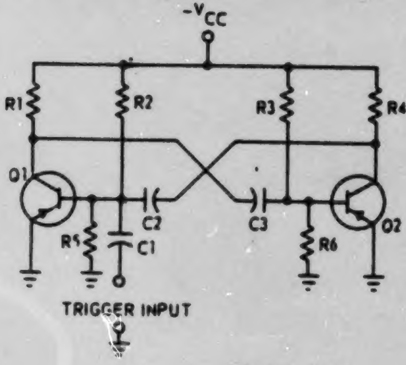
______ b. C1 open.

______ c. R3 open.

______ d. Q2 open.

MODULE SELF-CHECK

Questions 5 thru 7, refer to Figure 13 and Chart 10.



-VCC
R1
R2
R3
R4
Q1
C2
C3
Q2
R5
C1
R6
TRIGGER INPUT

Figure 13

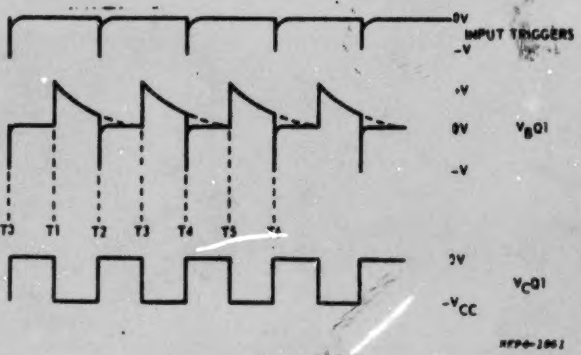


Chart 10

5. The circuit in Figure 13 is correctly identified as a (triggered, free-running) (Astable, Monostable, Bistable) multivibrator.

6. The purpose of using input triggers to this circuit is to

_______ a. increase pulse width.

_______ b. decrease pulse width.

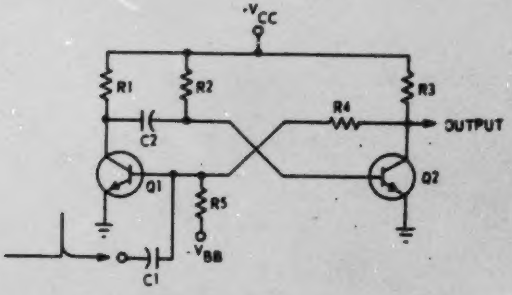
_______ c. impair frequency stability.

_______ d. improve frequency stability.

7. On Chart 10, the time from T1 to T3 is called__________ __________.

__________________; this time is controlled by the (trigger frequency, RC Time Constants).

Questions 8 through 12, refer to Figure 14 and Chart 11.



+VCC
R1
R2
R3
R4
OUTPUT
C2
Q1
Q2
R5
-VBB
C1

Figure 14

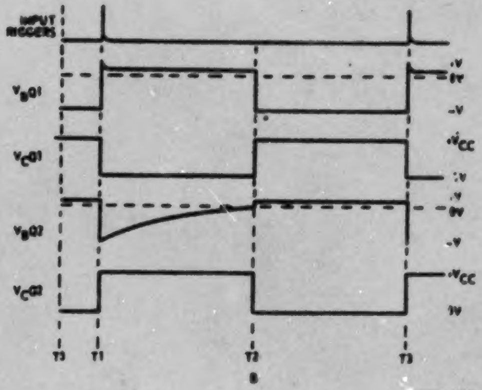


Chart 11

224

SOLID STATE MULTIVIBRATORS

1. SCOPE: There are three basic multivibrators that will be explained in this module. A complete circuit analysis of each type, including component purposes, waveshapes, uses, and troubleshooting procedures will be covered. You are expected to become familiar with each facet of development as it is covered. And, since the Schmitt Trigger circuit is very similar to multivibrators, it also is covered in this module to approximately the same depth. All of these circuits have numerous applications. In fact, regardless of your particular electronics specialty, you will no doubt encounter weapons systems requiring square wave generation, timing, and wave shaping. Multivibrators and Schmitt Trigger circuits perform all of these functions.

2. OBJECTIVES: Upon completion of this module you should be able to satisfy the following objectives:

a. Given schematic diagrams of the following solid state multivibrators, select the name and primary use of each:

(1) Astable.

(2) Monostable.

(3) Bistable.

b. Given the schematic diagram of a multivibrator and a list of statements, select the statement that describes the effects of time constants on pulse width, pulse recurrence frequency, and pulse recurrence time.

c. Given the schematic diagram of a multivibrator and a list of statements, select the statement that describes the effects of triggering on circuit operation.

d. Given a trainer with a malfunctioning multivibrator circuit, a schematic diagram, multimeter, and oscilloscope, determine the faulty component.

e. Given a schematic diagram of a Schmitt Trigger circuit and a list of symptoms, identify the faulty component.

AT THIS POINT, YOU MAY TAKE THE MODULE SELF-CHECK. IF YOU DECIDE NOT TO TAKE THE MODULE SELF-CHECK, TURN TO THE NEXT PAGE AND PREVIEW THE LIST OF RESOURCES. DO NOT HESITATE TO CONSULT YOUR INSTRUCTOR IF YOU HAVE ANY QUESTIONS.

LIST OF RESOURCES

SOLID STATE MULTIVIBRATORS

To satisfy the objectives of this module, you may choose, according to your training, experience, and preferences, any or all of the following:

READING MATERIALS:

Digest

Adjunct Guide with Student Text

LABORATORY EXERCISE:

Laboratory Exercise 47-1.

SELECT ONE OF THE RESOURCES AND BEGIN YOUR STUDY OR TAKE THE MODULE SELF-CHECK.

CONSULT YOUR INSTRUCTOR IF YOU REQUIRE ASSISTANCE.

SOLID STATE MULTIVIBRATORS

In general, multivibrators produce square or rectangular waveshapes in their output. They are used in numerous applications such as timing, gating, shaping, storing, shifting, and frequency division. Because of their numerous applications, three basic types are required. However, for specialized applications, the basic types are frequently modified as required to fit the specific need. The theory of operation of all types are very similar and, complete mastery of one will enable you to distinguish and understand individual differences.

Identification of the three basic types is relatively simple. Figure 1 represents a basic Astable; figure 2 is a basic Monostable, and figure 3 is a basic Bistable multivibrator. The output waveshapes of each are shown, along with the input tirgger if a trigger is required. Use these schematic diagrams and waveshapes while reading the explanations that follow.

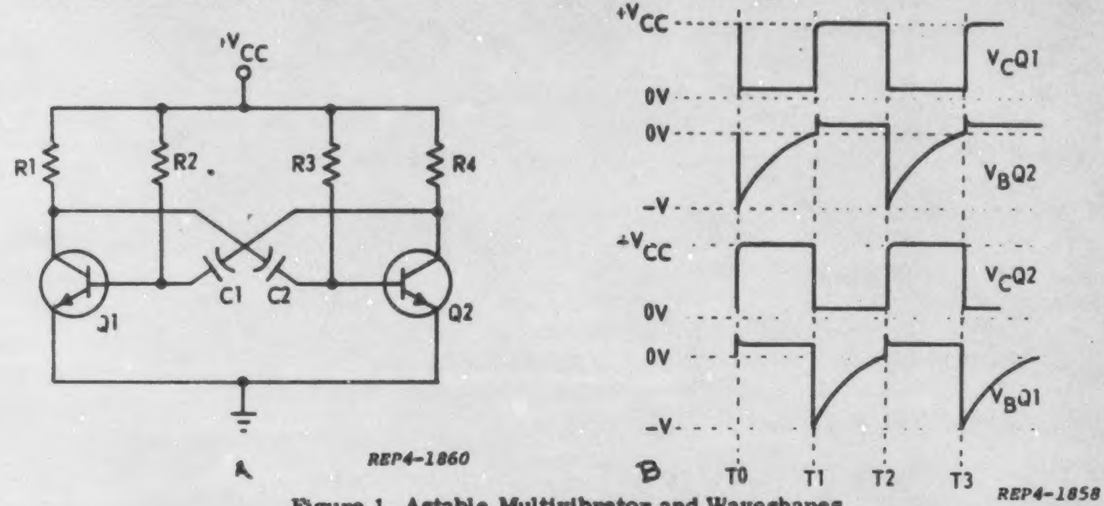

+VCC
R1
R2
R3
R4
C1
C2
Q1
Q2
REP4-1860
A
+VCC
0V
VCQ1
0V
-V
VBQ2
+VCC
0V
VCQ2
0V
-V
VBQ1
B
T0
T1
T2
T3
REP4-1858

Figure 1. Astable Multivibrator and Waveshapes

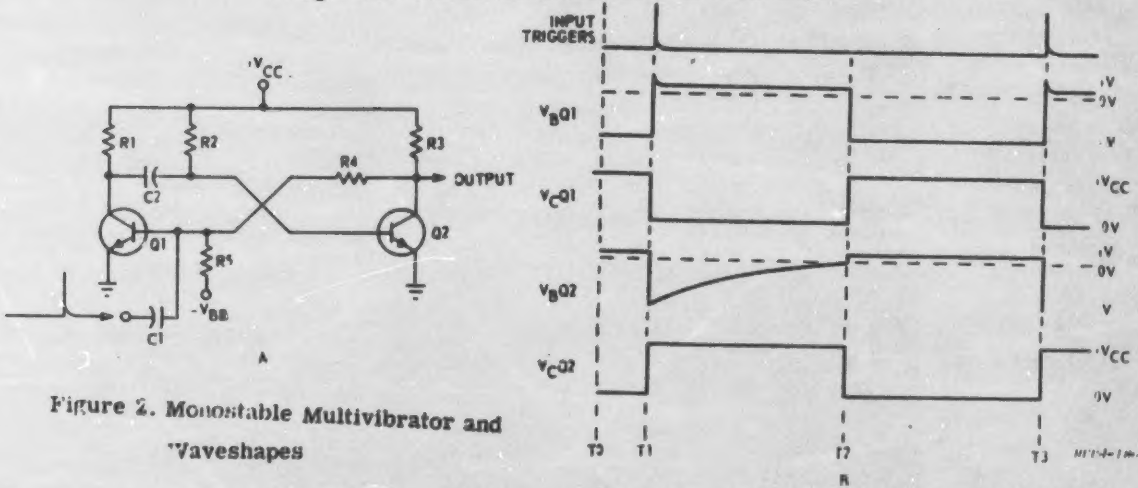

+VCC
R1
R2
R3
R4
C2
OUTPUT
Q1
Q2
R5
-VBB
C1
A
INPUT TRIGGERS
VBQ1
VCQ1
VBQ2
VCQ2
+V
0V
-V
+VCC
0V
+V
0V
-V
+VCC
0V
T0
T1
T2
T3
B

Figure 2. Monostable Multivibrator and Waveshapes

The names of the three basic multivibrators are derived from the number of stable states. For instance, the Astable has no stable state. Q1 and Q2 will alternately switch from cutoff to saturation; when Q1 is cutoff, due to the feedback, Q2 is saturated. The Monostable has one

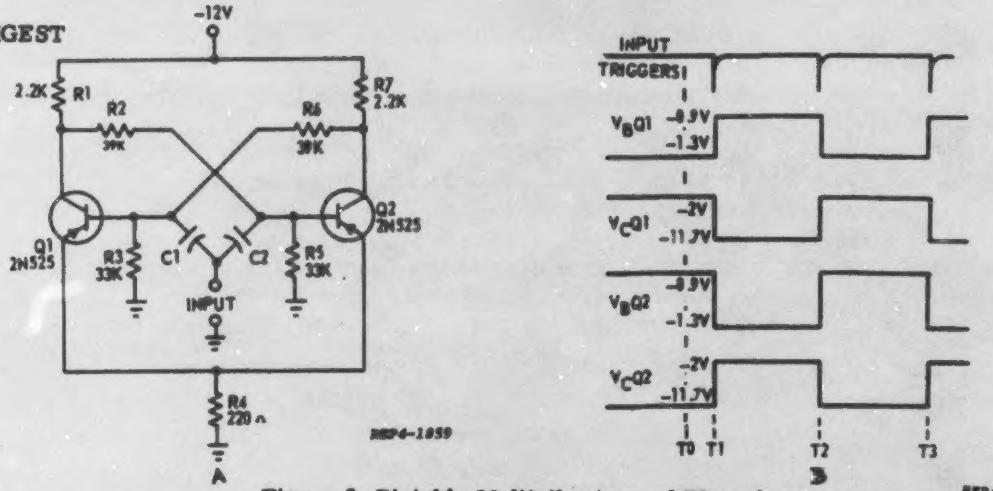


Figure 3. Bistable Multivibrator and Waveshapes

REP4-1865

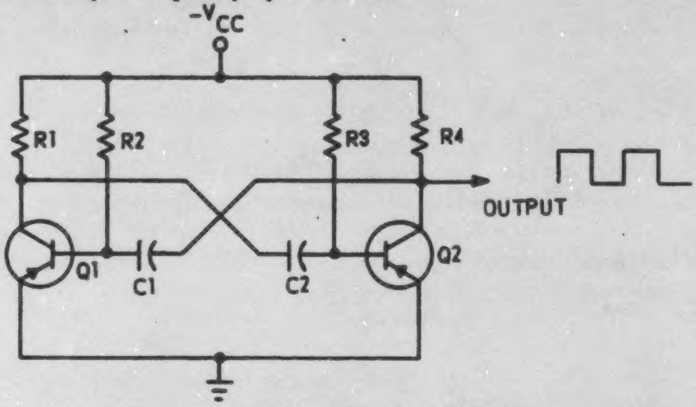
stable state. Due to the bias arrangement, one transistor will remain cutoff (in the figure 2 circuit, Q1) and the other will remain saturated until an external trigger is applied. The trigger will cause the cutoff transistor to saturate and the saturated transistor to cutoff (caused by feedback). After a period, determined by the RC time constant (R2 and C2 of figure 2), the circuit will return to the original state until the next trigger is applied. The Bistable, as the name implies, has two stable states. One transistor will be saturated and the other transistor cutoff until an external trigger is applied. The trigger causes the transistors to reverse states, and they will remain in the reverse state until a second trigger is applied to switch them back.

For circuit identification, (figure 1) note that the astable circuit has a resistor/capacitor combination in each base circuit, C2/R3 for Q2, and C1/R2 for Q1. The monostable has a resistor/capacitor combination (figure 2) in only one base circuit, R2/C2 for Q2. And, the bistable uses direct coupling from the collector to base of both transistors (figure 3). In addition, the bistable employs an emitter resistor that is common to both transistors (R4).

The waveshapes of each type multivibrator are valuable aids to understanding their operational characteristics. For instance, the waveshapes of the figure 1 Astable circuit show that Q1 is saturated (T0 to T1) while Q2 is cutoff. It also shows that Q2 is being held at cutoff by the negative signal on its base. Further, it shows that the voltage on the Q2 base decreases at an exponential rate, and Q2 again becomes saturated when the voltage decreases sufficiently. C2 discharging through R3 determines how long Q2 stays cutoff. C1 discharging through R2 determines how long Q1 remains cutoff (T1 to T2). Now, the cutoff time of Q2, added to the cutoff time of Q1 produces one complete cycle (T0 to T2). Therefore, you should surmise that the output PRF is controlled by the base RC components (R2, C1, R3, C2). You should also see that a square wave could be taken from the collector of either (or both) transistors. The two signals are 180 degrees out of phase.

From the astable multivibrator waveshapes it should be evident that, if the location of either waveshape is given, the location of the other three is very simple to determine. Note that both transistors are common emitter configurations; therefore, a phase shift of 180 degrees will take place between the base and collector of each. Since the base circuits have RC time constants determining their waveshapes, they will have an exponential curve. So, if you were given the waveshape for VBQ2, for example, you would know that VBQ1 is exactly the same but 180 degrees out of phase. You would know that VCQ2 is a square wave that is 180 degrees out of phase with VBQ2. VCQ1 would be the same as VCQ2, but 180 degrees out of phase.

The waveshapes for the monostable and bistable circuits are equally as simple to determine. However, you should note that the monostable circuit has an exponential base circuit waveform on only one transistor, and the bistable circuit has square waves throughout. You should also note in the monostable circuit that the pulse width (T1 to T2) is controlled by the size of C2 and R2, but the output PRT (T1 to T3) is controlled by the input trigger. Both the pulse width (T1 to T2) and PRT (T1 to T3) of the bistable circuit is controlled by the input trigger. Further, in the bistable circuit, it takes two triggers in to produce one cycle out. Therefore, the bistable circuit divides the input frequency by two.



REP4-1864

Figure 4. PNP Astable Multivibrator

Troubleshooting multivibrator circuits (see figure 4) is relatively simple if you have learned and retained the basic concepts of transistor amplifiers. For instance, you should recall that increasing forward bias on a transistor decreases the transistor's resistance and increases the current flowing through it. If the forward bias is increased enough, the transistor will become saturated, lowering its total resistance drastically. When saturation occurs, the voltage from collector to ground (V_C) very nearly equals zero volts.

On the other hand, decreasing forward bias on a transistor increases its resistance and decreases the current through it. If the bias is decreased enough, a point is reached that forward bias becomes reverse bias, and the transistor is cutoff. When cutoff is reached, resistance of the transistor is maximum and current almost ceases to flow through it. Therefore, at cutoff, the collector to ground (V_C) voltage is nearly equal to V_{CC}.

Understanding the effects of bias changes is imperative to your comprehension of the following troubleshooting discussion:

Symptom: V_C of Q1 is nearly equal to V_{CC} and V_C of Q2 is nearly equal to zero volts. (See figure 4).

DIGEST

Cause: The symptom indicates that Q1 is at cutoff and Q2 is saturated. What would cause this? One possibility is R2 open. To understand this, trace the forward bias current path for Q1, from $-V_{CC}$, through R2, through the emitter/base junction, to ground. So, with R2 open, Q1 would have no forward bias; it would be cutoff, and its collector voltage (V_C) would very nearly equal V_{CC}. V_{CC} would be coupled from Q1 collector to Q2 base, causing Q2 to be saturated, and its V_C to nearly equal zero volts.

Q1 open would also cause this symptom. Remember that applied voltage (in this case V_{CC}) is dropped across an open. V_{CC} (from the collector of Q1) would be coupled to the base of Q2, keeping it saturated and its collector volage nearly equal to zero volts.

Symptom: V_C Q1 is nearly equal to zero volts; V_C Q2 is nearly equal to V_{CC}.

Cause: R3 open or Q2 open. If required, you can explain this to yourself by following the explanation for the symptom above, substituting Q2 for Q1, Q1 for Q2, R3 for R2, and R2 for R3.

Symptom: V_C Q1 equals zero volts; V_C Q2 is very low but greater than zero volts.

Cause: R1 open or Q1 shorted would cause this symptom. R1 and Q1 are in series; and, with R1 open, total voltage would be dropped across R1, leaving none to be dropped between the Q1 collector and ground. With Q1 shorted, its resistance would be zero ohms and would drop no voltage from collector to ground. But, how would this cause Q2 to be saturated, keeping its collector voltage near zero volts? The answer; it wouldn't. Recall that the only thing that will cause Q2 to decrease in conduction (and cutoff) is a changing voltage coupled to its base from the collector of Q1. Since the collector of Q1 is remaining at zero volts, C2 can not charge and discharge; so, nothing is coupled from the Q1 collector to Q2 base. Therefore, since Q2 has a constant forward bias from $-V_{CC}$, through R3, through the emitter/base junction to ground, it will conduct constantly near saturation, keeping V_C Q2 near zero volts.

Symptom: V_C Q2 and V_C Q1 is very low but greater than zero volts.

Cause: C1 open or C2 open. Consider that C1 is open and follow along. When power is first applied, both transistors initially conduct almost at saturation; therefore, the V_C of both will be low. Now, with C1 open, nothing will be coupled from the collector of Q2 to the base of Q1. So, the V_C of Q1 will stabilize at a value determined solely by the amount of forward bias current that flows through R2 and the emitter/base junction. Since V_C of Q1 will not be changing, nothing will be coupled to the base of Q2. Therefore, V_C Q2 will be determined solely by the forward bias current that flows through R3 and the emitter/base junction. Since the value of R2 and R3 is chosen to cause the transistors to conduct near saturation, V_C of both will be very low. By substituting C2 for C1 and Q2 for Q1, you can, if necessary, go through the same explanation for C2 open.

Symptom: V_C Q1 equals V_{CC}; V_C Q2 nearly equals zero volts.

Cause: R1 shorted, Recall that no voltage is dropped across a shorted component (R1 in this case), and since R1 and Q1 are in series between $-V_{CC}$ and ground, V_{CC} would be measured on the Q1 collector. This voltage would be coupled to the base of Q2, keeping it saturated, and its collector voltage nearly equal to zero volts.

Symptom: V_C Q2 equals V_{CC}; V_C Q1 nearly equals zero volts.

Cause: R4 shorted. If necessary, you can explain this malfunction by following the preceeding explanation, substituting R4 for R1, Q2 for Q1, and Q1 for Q2.

Before discussing the following malfunctions, a brief review is in order. Recall that increasing forward bias of a transistor beyond a given point (depending on the transistor's characteristics) will cause structural breakdown and destruction of the transistor. In all probability, structural breakdown would occur if either of the base components (C1 and R2 for Q1, and C2 and R3 for Q2) became shorted. However, for explanation, you can assume that the transistors can stand the added current without structural breakdown. Do so for the following discussion:

Symptom: V_C Q1 and V_C Q2 nearly equal to zero.

Cause: C1, C2, R2, or R3 shorted. You should see that parallel paths now exist for forward bias current; from $-V_{CC}$ through R2 and from $-V_{CC}$ through R4 and around the shorted C1. These two currents combine as the base/emitter current for Q1, causing V_C Q1 to be very near zero. And, since the voltage does not change, nothing is coupled to Q2 to affect its operation. Since R3 allows enough current to flow through the emitter/base junction of Q2 to cause saturation, its collector voltage also will be near zero. Either of the other three base circuit components shorted will cause basically the same operation.

If you thoroughly understand the troubleshooting of the astable circuit as explained above, you should be able to apply this knowledge in troubleshooting the monostable and bistable circuits.

If the waveshape of a square wave signal degenerates to the point that is rounded, a "Schmitt Trigger" circuit may be used. The circuit will furnish a sharp rectangular output pulse of about the same duration and phase as the input signal. The Schmitt Trigger restores a degenerated pulse to its original shape.

The Schmitt trigger is basically a multivibrator. The main difference is that one of the coupling networks is replaced by a common emitter resistor, providing additional regenerative feedback to obtain a faster switching time. The circuit is shown in Figure 5.

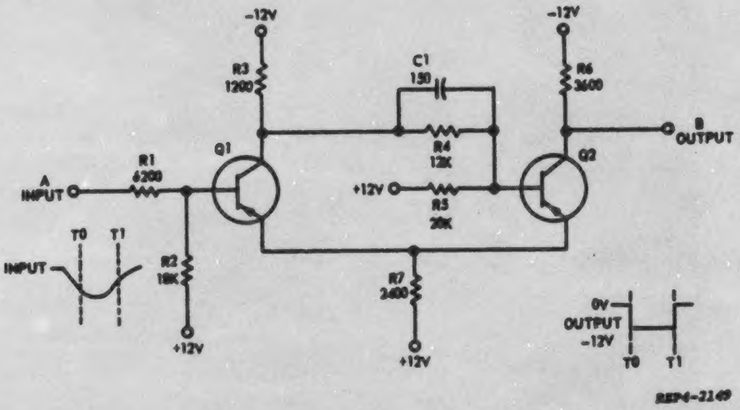


Figure 5. Schmitt Trigger

DIGEST

In the quiescent state, the input to the Schmitt trigger circuit is at 0 volts. Q1 is cut off, and Q2 is held at saturation by the negative voltage developed across the voltage dividing network R5, R4, and R3. The current through Q2 causes a voltage drop across R7, reverse biasing Q1 and keeping it cut off. In this condition, the output taken from the collector of Q2 is about 0 volts.

At T_0, the negative signal applied to input A has sufficient amplitude to turn Q1 on. The collector of Q1 goes to about 0 volts as the transistor conducts. This negative change is coupled to the base of Q2 causing a decrease in conduction. The decrease in the conduction of Q2 through R7 reduces the reverse bias on Q1. Q1 is now saturated, and Q2 is cutoff. The voltage out of Q2 is almost equal to V_{CC}.

The circuit remains in this state until T1 when the input voltage becomes less negative. When the input signal swings in the positive direction, Q1 will start to conduct less. The collector voltage of Q1 will start to conduct less. The collector voltage of Q1 starts in the negative direction. This change is coupled to the base of Q2 and turns it on. The increase in current through Q2 and R7 puts reverse bias on Q1, cutting it off. The collector of Q1 goes to negative V_{CC}, and Q2 conducts near saturation. The output is near 0 volts.

Notice how the rounded input wave is converted to a square wave output. The sharp rise and fall of the edges is due to the regenerative feedback between Q2 and Q1. Any slight change in the conduction of Q1 is applied to the base of Q2 which changes the emitter voltage of Q1. Capacitor C1 speeds the transition from one state to the other.

Schmitt trigger circuits are not only used for squaring circuits but also as voltage-level sensing circuits. Voltage sensing circuits are useful in warning or control circuitry. If the input voltage rises above or falls below a specified level, the Schmitt circuit produces an output. The output then activates a warning device.

The troubleshooting theory of the Schmitt Trigger circuit is very similar to the astable multivibrator; therefore, the following symptoms and probable causes are given without explanation. Refer to Figure 5 while following the troubles and causes.

Symptom: No output; V_C Q2 is near zero.

Possible Causes: R3, R4, or C1 shorted.

Symptom: V_C Q2 is normal; no output.

Possible Causes: R1 or Q1 open; R2 shorted.

Symptom: High frequency distortion in output.

Possible Cause: C1 open.

YOU MAY STUDY ANOTHER RESOURCE OR TAKE THE MODULE SELF-CHECK.

SOLID STATE MULTIVIBRATORS

INSTRUCTIONS:

Study the referenced materials as directed.

Return to this guide and answer the questions.

Check your answers against the answers at the top of the next even numbered page following the questions.

If you experience any difficulty, contact your instructor.

Begin the program.

To date, with exception of the blocking oscillator, you have been concerned with circuits that either create or amplify sine wave signals. However, in electronics the requirement often exists for signals other than sine wave. For instance, you should recall that a pulsed oscillator required a square or rectangular wave input. The input wave turned the oscillator on for a specific period, and then turned it off for a specific period. The circuits used to generate these square and rectangular waves are called multivibrators.

Square and rectangular wave signals possess characteristics not found in sine wave signals. Consequently, different terms are required for designating these characteristics. And, a discussion of these terms is necessary prior to learning how they are generated. How well you understand the circuits will, to a great degree, depend upon your mastery of the square and rectangular wave charactdristics.

A. Turn to Student Text, Volume VI, and study paragraphs 5-1 through 5-24. Return to this page and answer the following statements/questions.

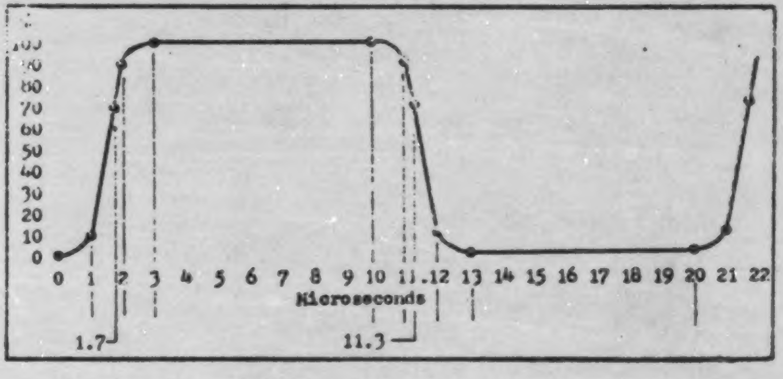


Chart 1

ADJUNCT GUIDE

1. Refer to Chart 1 and complete the following blanks:

a. Pulse Width = ______________________ microsecond(s).

b. Rise Time = ______________________ microsecond(s).

c. Fall Time = ______________________ microsecond(s).

d. PRT = ______________________ microsecond(s).

e. PRF = ______________________ kHz

2. The waveform of Chart 1 is a (square) (rectangular) wave; decreasing the width of the positive alternation by 10 microseconds and increasing the width of the negative alternation by 10 microseconds would change it to a (square) (rectangular) wave, and would cause (an increase) (a decrease) (no change) in PRT, and (an increase) (a decrease) (no change) in PRF.

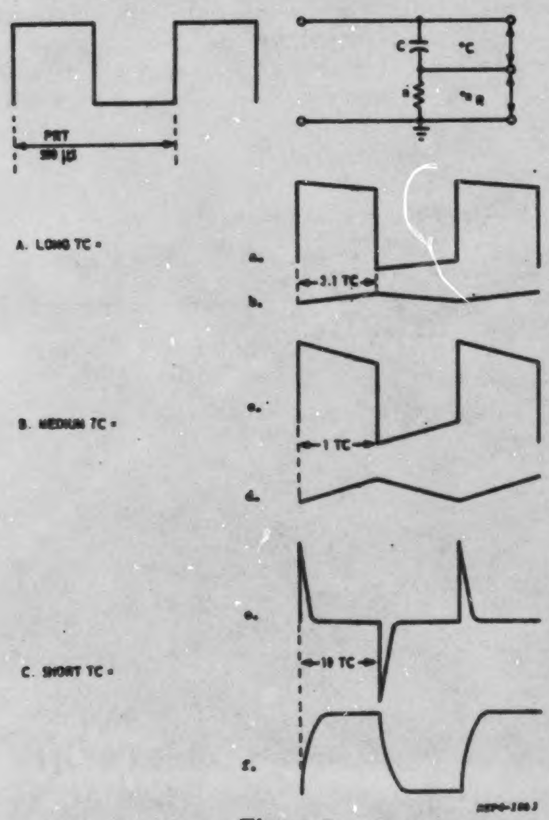

PRT
µs
C
e_C
R
e_R
A. LONG TC =
a.
0.1 TC
b.
B. MEDIUM TC =
c.
1 TC
d.
C. SHORT TC =
e.
10 TC
f.

Figure 6

3. Given the RC circuit with square wave input and the associated output waveforms (a through f) in Figure 6, label the output waveshapes as being taken across the resistor (E_R) or the capacitor (E_C).

a.

b.

c.

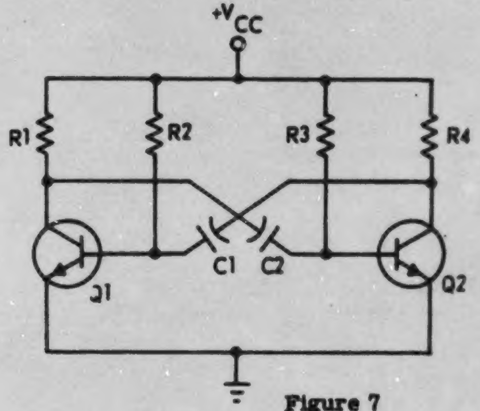
d.

e.

f.

CONFIRM YOUR ANSWERS ON THE NEXT EVEN NUMBERED PAGE.

B. Turn to Student Text, Volume VI, and study paragraphs 5-25 through 5-38. Return to this page and answer the following statements/questions.



REP4-1860

Figure 7

1. Figure 7 is the schematic diagram of a/an ________________ multivibrator.

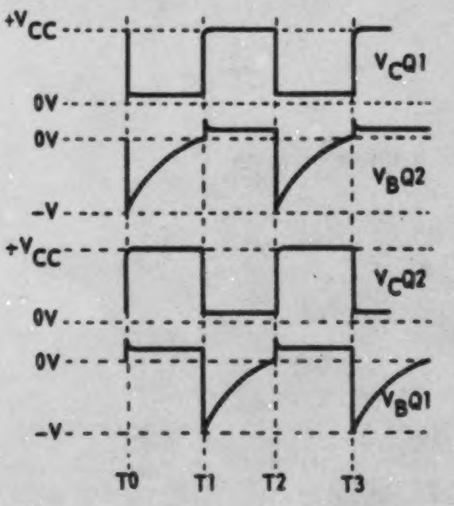
ANSWERS TO A:

1. a. Pulse width = 9.6 microseconds.
   b. Rise Time = 1 microsecond.
   c. Fall time = 1 microsecond.
   d. PRT = 20 microseconds.
   e. PRF = 50 kHz.

2. square, rectangular, no change, no change

3. a. ER
   b. EC
   c. ER
   d. EC
   e. ER
   f. EC

If you missed ANY questions, review the material before you continue.



+VCC
0V
VCQ1
0V
VBQ2
-V
+VCC
0V
VCQ2
0V
VBQ1
-V
T0
T1
T2
T3

REP4-1858

Chart 2

2. Given Chart 2 as the waveshapes of the Figure 7 circuit, with waveshape "B" labeled as VBQ2, label the remaining waveshapes.

A. ______________________________

C. ______________________________

D. ______________________________

For questions 3 through 8, refer to Figure 7 and Chart 2 as necessary.

3. The time from T1 to T2 of waveform "D" is primarily determined by the values of C __________ and R __________ .

4. List the four components that are the primary determinants of the PRT and PRF of the Figure 7 circuit.

A. ______________________________

B. ______________________________

C. ______________________________

D. ______________________________

5. Refer to waveform "A" of Chart 2. The width of the square wave between T2 and T3 could be incresed by

______ a. increasing the value of C2.

______ b. decreasing the value of R3.

______ c. increasing the value of C1.

______ d. increasing the value of R2.

6. Symptom: VCQ1 very nearly equals V_{CC}; VCQ2 very nearly equals zero. A possible trouble is

______ a. R3 open.

______ b. R2 open.

______ c. R1 open.

______ d. R4 open.

7. If C1 should become open, which of the following conditions would exist?

______ a. VCQ1 and VCQ2 would be higher than normal.

______ b. VCQ1 would be high and VCQ2 would be low.

______ c. VCQ2 would be high and VCQ1 would be low.

______ d. VCQ1 and VCQ2 would be lower than normal.

8. (Increasing) (Decreasing) the values of R2, R3, C1 and C2 would cause the output PRT to increase and output PRF to (increase) (decrease).

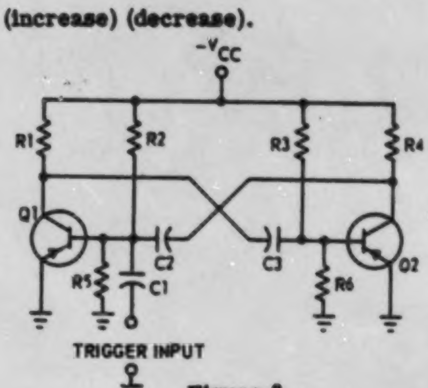


Figure 8

9. The Figure 8 schematic diagram represents a/an ______________________________. multivibrator; its output frequency is controlled by the (input trigger frequency) (RC time constants).

10. For proper operation of the Figure 8 circuit, the input trigger frequency must be slightly (higher) (lower) than the free running frequency.

11. Pulse width (cutoff time of Q1) of the output signal from the figure 8 circuit is controlled by the (trigger PRT) (RC time constants).

12. If C1 of the Figure 8 circuit became open, which of the following conditions would exist?

______ a. Q1 would remain at cutoff and Q2 would remain at saturation.

______ b. Q2 would remain at cutoff and Q1 would remain at saturation.

______ c. The circuit wuld continue to function, but at a slightly lower frequency.

______ d. The circuit would continue to function, but at a slightly higher frequency.

CONFIRM YOUR ANSWERS ON THE NEXT EVEN NUMBERED PAGE.

C. Turn to Student Text, Volume VI, and study paragraphs 5-40 through 5-48. Return to this page and answer the following statements/questions.

For questions 1 through 6, refer to Figure 9 and Chart 3 as necessary.

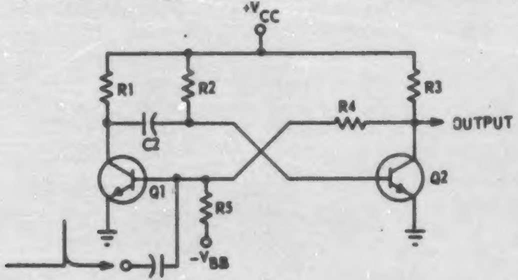


Figure 9

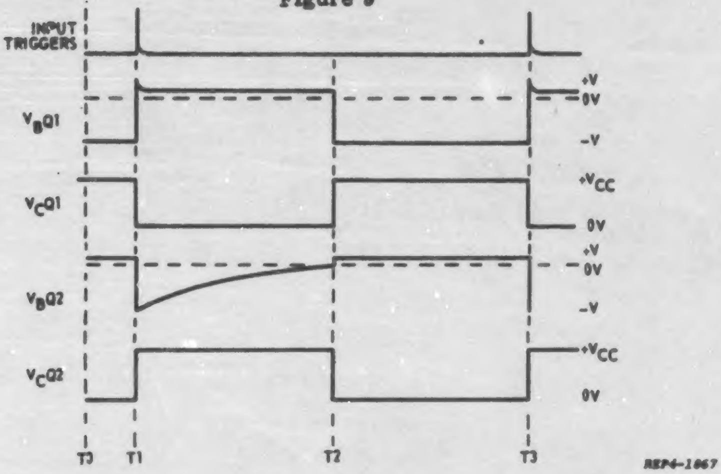


Chart 3

1. Figure 9 is the schematic diagram of a ______________________________;

before triggers are applied, Q ____ is saturated and Q ____ is cutoff.

2. Given Chart 3 as the waveshapes for the Figure 9 circuit, with waveshape "B" labeled as VCQ1, label the remaining waveshapes.

A. ______________________________

C. ______________________________

D. ______________________________

3. An open R ____ would remove forward bias from Q2.

4. Output PRT of the Figure 9 circuit is controlled by the (input trigger PRT) (value of C2 and R2), and output pulse width is controlled by the (input trigger PRT) (value of C2 and R2).

ANSWERS TO B:

1. astable
2. A. VCQ1

   C. VCQ2

   D. VBQ1
3. C1 and R2
4. A. R2

   B. R3

   C. C1

   D. C2
5. a
6. b
7. d
8. Increasing, decrease
9. triggered astable, input trigger frequency
10. higher
11. RC time constants
12. c

If you missed ANY questions, review the material before you continue.

5. Refer to waveform "D" of Chart 3. The time from T1 to T2 could be increased by

______ a. increasing the value of R2.

______ b. increasing the trigger PRT.

______ c. decreasing the value of R2.

______ d. decreasing the trigger PRT.

6. If C1 (figure 9) became open, which of the following conditions would exist?

_______a. VCQ2 would remain high and VCQ1 would remain low.

_______b. VCQ1 would remain high and VCQ2 would remain low.

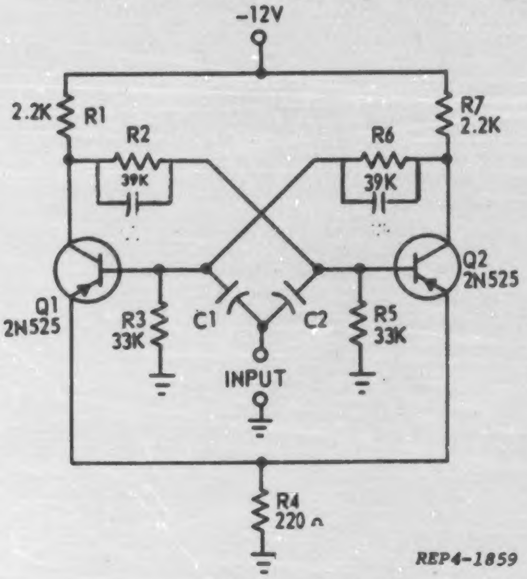
_______c. The circuit would continue to function, but at a slightly lower frequency.

_______d. The circuit would continue to function, but at a slightly higher frequency.

CONFIRM YOUR ANSWERS ON THE NEXT EVEN NUMBERED PAGE.

D. Turn to Student Text, Volume VI, and study paragraphs 5-49 through 5-59. Return to this page and answer the following statements/questions.

For questions 1 through 13, refer to Figure 10 and Chart 4 as necessary.



REP4-1859

Figure 10

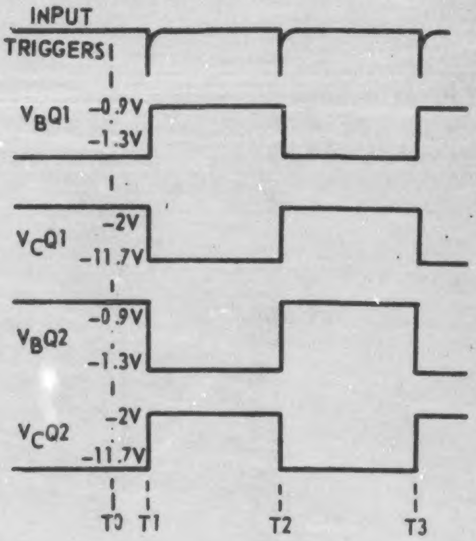


Chart 4

REP4-1865

1. The Figure 10 schematic diagram is correctly identified as a/an ____________________

____________________ multivibrator.

2. Given Chart 4 as the waveshapes for the Figure 10 circuit with waveshape "A" labeled as VBQ1, label the remaining waveshapes.

B. ______________________________

C. ______________________________

D. ______________________________

ANSWERS TO C:

1. Monostable Multivibrator; Q2, Q1

2. A. VBQ1

   C. VBQ2

   D. VCQ2

3. R2

4. input trigger PRT, value of C2 and R2

5. a

6. b

If you missed ANY questions, review the material before you continue.

3. The output PRF of this circuit is controlled by the (input trigger PRF) (RC time constants), and the output pulse width is controlled by the (input trigger PRT) (RC time constants).

4. Complete the following equations:

   a. IR7 = IC Q2 + IR ____

   b. IR4 = (IR1 - IR5) + (IR7 - ____)

   c. V_{CC} = ER1 + ER2 + ER ____

5. Given: The PRT of the input trigger to the Figure 10 circuit is 500 microseconds. The PRF of the output is ____________ kHz.

6. Which of the following is the path through which forward bias CURRENT for Q2 will flow?

   ____ a. -V_{CC}, R7, collector, emitter, R4, ground.

   ____ b. -V_{CC}, R7, R6, R3, ground.

   ____ c. -V_{CC}, R1, R2, R5, ground.

   ____ d. -V_{CC}, R1, R2, base, emitter, R4, ground.

7. Increasing the PRT of the input triggers would cause the output pulse width

_______a. and output frequency to increase.

_______b. to increase and output frequency to decrease.

_______c. to decrease and output frequency to increse.

_______d. to decrease and output frequency to decrease.

8. The primary purpose of C3 and C4 is to

_______a. filter the forward bias for Q2 and Q1.

_______b. improve the circuit's low frequency response.

_______c. improve the circuit's high frequency response.

_______d. prevent DC coupling between the 2 transistors.

9. If C1 became open, which of the following conditions would exist?

_______a. Q1 would be saturated and Q2 cutoff.

_______b. Q1 would be cutoff and Q2 saturated.

_______c. Q1 and Q2 would be cutoff.

_______d. Q1 and Q2 wouldabe saturated.

10. Symptom: VCQ1 and VCQ2 very nearly equals $V_{CC.}$ A possible trouble is

_______a. C2 open.

_______b. R1 and R7 open.

_______c. R4 open

_______d. R2 open.

11. If R2 became open, which of the following conditions would exist.

_______a. Q2 would be cutoff, but would conduct briefly each time a negative trigger is applied to its base.

_______b. Q1 would be cutoff, but would conduct briefly each time a negative trigger is applied to its base.

_______c. Q2 would be saturated, but would cutoff briefly each time a negative trigger is applied to its base.

ADJUNCT GUIDE

12. An open R5 would cause forward bias on Q2 to (increase) (decrease) and forward bias on Q1 to (increase) (decrease)

13. The leading edge on the output signal from Q2 is rounded. A possible cause of this is that

______a. C4 is open.

______b. C3 is open.

______c. C1 is open.

______d. C2 is open.

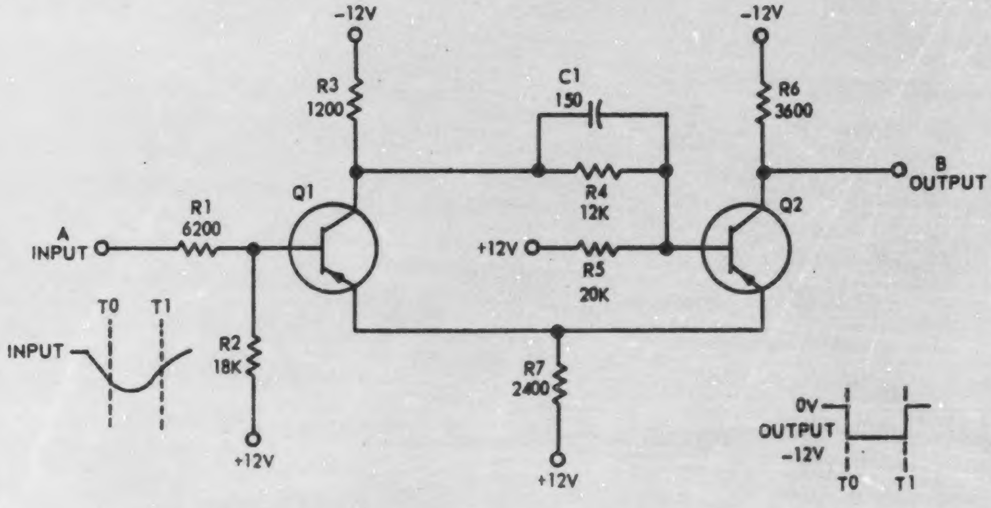
CONFIRM YOUR ANSWERS ON THE NEXT EVEN NUMBERED PAGE.

E. Turn to Laboratory Exercise 47-1. This exercise will reinforce and prove most of the principles you have learned about multivibrators. In addition, you will gain valuable experience in the practical aspects of multivibrator troubleshooting.

Return and continue with this program when the Laboratory Exercise has been completed.

F. Turn to Student Text, Volume VI, and study paragraphs 5-60 to 5-71.
Return to this page and answer the following statements/questions:

For questions 1 through 5, refer to the Figure 11 schematic diagram as necessary.


-12V
-12V
R3
1200
C1
150
R6
3600
B
OUTPUT
Q1
R4
12K
Q2
R1
6200
A
INPUT
+12V
R5
20K
T0
T1
INPUT
R2
18K
R7
2400
+12V
+12V
0V
OUTPUT
-12V
T0
T1

REP4-2149

Figure 11

1. The Figure 11 schematic diagram is correctly identified as a/an

_______a. free running bistable multivibrator.

_______b. triggered astable multivibrator.

_______c. Schmitt Trigger circuit.

_______d. pulse shaping monostable multivibrator.

2. With no input signal to the Figure 11 circuit, Q1 is (cutoff) (saturated), and the Q2 output is (0 volts) ($-V_{CC}$).

3. The two principal purposes of the Figure 11 circuit are wave ____________________ and voltage level ____________________ .

4. Symptoms: Circuit has no output; V_C Q2 is normal. A possible trouble is

_______a. R2 open.

_______b. R1 open.

_______c. R3 open.

_______d. R4 open.

5. Symptoms: Output signal is distorted at high frequencies. VC Q1 and VC Q2 are normal. A possible trouble is

_______a. C1 shorted.

_______b. C1 open.

_______c. R4 open.

_______d. R4 shorted.

CONFIRM YOUR ANSWERS ON THE NEXT EVEN NUMBERED PAGE.

ADJUNCT GUIDE

ANSWERS TO D:

1. Bistable
2. B. VCQ1
   C. VBQ2
   D. VCQ2
3. input trigger PRF, input trigger PRT
4. a. $IR7 = IC\ Q2 + IR\ \underline{6}$
   b. $IR4 = (IR1 - IR5) + (IR7 - IR\underline{3})$
   c. $V_{CC} = ER1 + ER2 + ER\underline{5}$
5. 1 kHz
6. d
7. b
8. c
9. b
10. c
11. a
12. increase, decrease
13. b

If you missed ANY questions, review the material before you continue.

ANSWERS TO F:

1. c
2. cutoff, 0 volts
3. shaping, sensing
4. b
5. b

If you missed ANY questions, review the material before you continue.

YOU MAY STUDY ANOTHER RESOURCE OR TAKE THE MODULE SELF-CHECK.

47-1

SOLID STATE MULTIVIBRATORS

OBJECTIVES:

1. Given a trainer having a semiconductor multivibrator circuit, multimeter, and oscilloscope, measure the output amplitude and frequency within ± 10 percent accuracy.

2. Given a trainer with a malfunctioning multivibrator circuit, a schematic diagram, multimeter, and oscilloscope, determine the faulty component.

EQUIPMENT:

1. Sweep Generator Trainer (DD-5932)
2. Oscilloscope (LA-261)
3. Transistor Power Supply (DD-4649)
4. Multimeter (PSM-6)

REFERENCE: Student Text, Volume 6, paragraphs 5-22 thru 5-59

CAUTION: OBSERVE BOTH PERSONNEL AND EQUIPMENT SAFETY AT ALL TIMES. REMOVE WATCHES AND RINGS.

PROCEDURES: 1. Equipment Preparation

a. Oscilloscope Controls — Position

	Oscilloscope Controls	Position
(1)	Turn POWER	ON
(2)	MODE	Alternate
(3)	POLARITY	Normal DC
(4)	VOLTS/DIV	
	"A" Channel	1 Calibrated (Change as required)
	"B" Channel	.5 calibrated (Change as required)
(5)	TIME/DIV	.5 milliseconds
(6)	TRIGGER SELECTOR	Auto, Ext, +
(7)	HORIZONTAL POSITION	Adjust for Normal Sweep
(8)	FOCUS + INTENSITY	Adjust for Clear Presentation

b. Interconnections

1. Ground Oscilloscope to Trainer at TP2.
2. Connect Trigger input to TP11 of Trainer.
3. Connect Power Supply to Trainer (Use Jones Plug cable).

c. Transistor Power Supply

(1) On/Off Switch - On
(2) Adjust voltage to 25 volts (Use Built-in meter).

d. Trainer

(NOTE: The student WILL NOT, at any time, open the hinged panel on back of trainer.)

(1) S1 - R11
(2) S2 - C5
(3) S4 - Down
(4) S3 - R12

Consult your instructor, and let him ensure that the trainer is in its normal operating condition.

2. Trainer Analysis

Transistors Q2 and Q3, along with associated components, comprise a monostable multivibrator. A trigger for the multivibrator is supplied by Q1 and its associated components. Q4 and its associated components will be used in a later lab project. This trainer provides a simple, practical method for your use in learning the operational theory of multivibrators in general, and monostable multivibrators in particular. This trainer will also give you valuable experience in the practical aspects of multivibrator troubleshooting.

3. Activity

(NOTE: The multimeter will be used on the ohmmeter function when an open or shorted component is suspected, and the oscilloscope will be used for measuring DC voltages in this project).

a. Establish a 0 volts DC reference for "A" Channel on the bottom line of the oscilloscope, and 0 volts DC reference for "B" Channel on the center line. Connect "A" Channel probe to TP 3 and "B" Channel probe to TP5. Read and record the amplitude of the signal at each test point.

TP3 ________________ V Pk.

TP5 ________________ V Pk.

b. Read and record the pulse recurrence time (PRT) of the trigger signal appearing at TP3. Calculate and record the PRF.

PRT ________________ milliseconds

PRF ________________ Hz

c. Draw the signal appearing at TP3 and TP5 on Chart 5 below. (NOTE: Draw the first trigger pulse (TP3) at the .5 milliseconds line.)

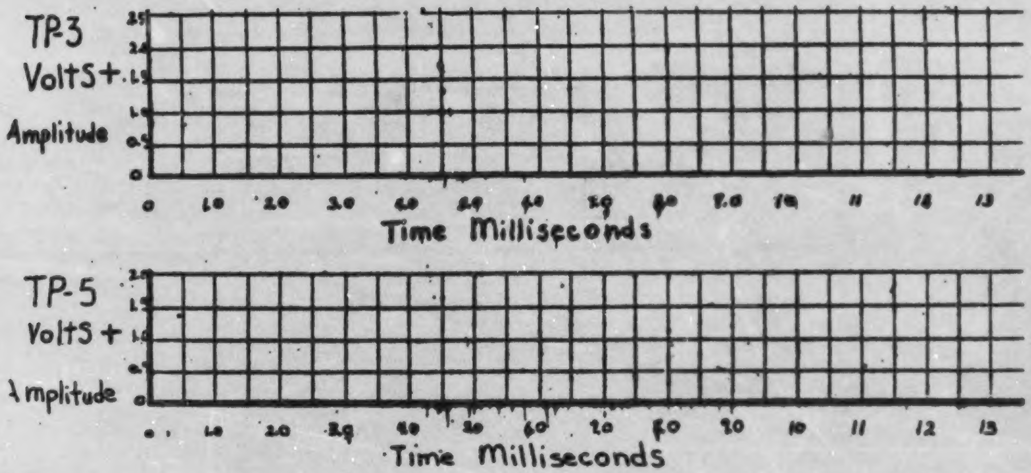


Chart 5

d. Move "B" Channel probe to TP4, and draw the signal appearing there on the chart below.

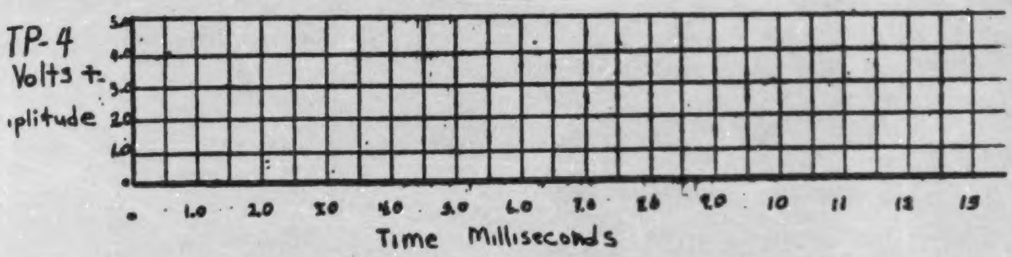


Chart 6

e. Move "B" Channel probe to TP6, and draw the signal appearing there on the chart below.

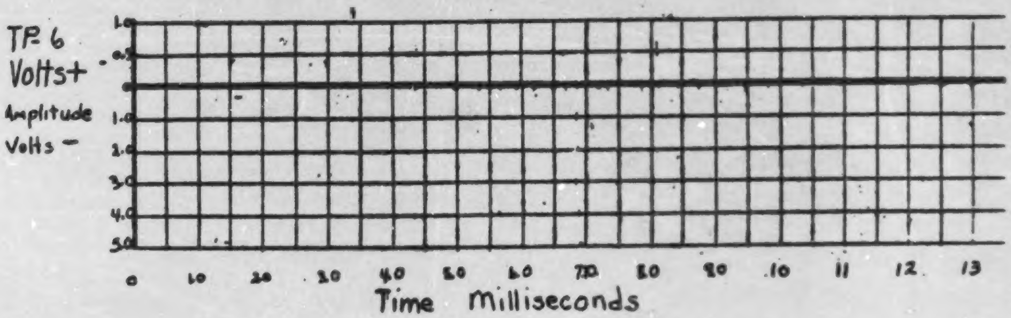


Chart 7

LABORATORY EXERCISE

f. Move "B" Channel probe to TP7, and draw the signal appearing there on the chart below.

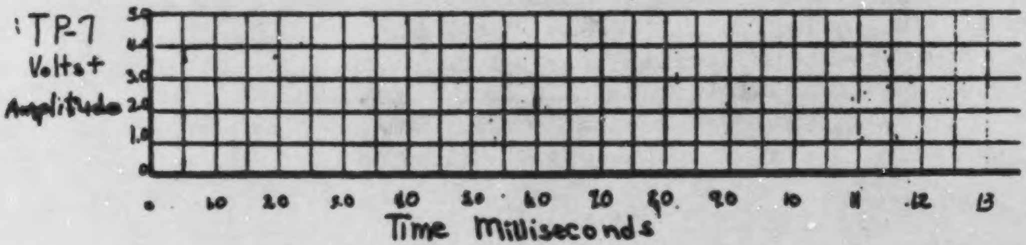


Chart 8

g. Underline the correct response to the following statements:

(1) When thetrigger is applied to the base of Q2, Q2 is driven into (saturation, cutoff) and Q3 is driven into (cutoff, saturation).

(2) The PRT of the output signal is being controlled by the (trigger PRT, value of R5 and C3).

(3) The frequency of the multivibrator is (the same as, one-half) the frequency of the trigger.

(4) During the time the voltage on the base of Q3 is negative, Q3 is (saturated, cutoff) and Q2 is (saturated, cutoff).

(5) The signals on the collectors of Q2 and Q3 are (in, 180 degrees out of) phase with each other.

(6) The signals on the bases of Q2 (TP5) and Q3 (TP6) are (in, 180 degrees out of) phase with each other.

(7) The signal on the base of Q2 (TP5) is (in, 180 degrees out of) phase with the signal on the collector of Q3 (TP7).

h. Refer to chart and read and record the pulse width and rest time of the signal at TP7. (NOTE: Consider the negative going pulse as rest time, and the positive going pulse as pulse width.)

Rest Time __________ milliseconds.

Pulse Width __________ milliseconds.

i. Consult your instructor and have him insert trouble number one.

j. Using "B" Channel probe, read the rest time (negative going) and pulse width (positive going) of the signal at TP7, and record below.

Rest Time________________ milliseconds.

Pulse Width ________________ milliseconds.

Underline the correct response to the following statements:

(1) Cutoff time of Q3 has (increased, decreased) and cutoff time of Q2 has (increased, decreased).

(2) The pulse width (positive going portion of signal) at TP7 has (increased, decreased).

(3) A trouble that could possibly cause the above symptom is that:

(a) the trigger frequency has increased.
(b) the trigger frequency has decrased.
(c) R5 has increased.
(d) R5 has decreased.

k. Consult your instructor and have him remove trouble number one and insert trouble number two.

l. Move sync lead to TP3. Leave "A" Channel probe in TP5, and use "B" Channel probe to check the amplitude of the voltage at TP4, TP6, and TP7. Record the results below:

TP4________________ volts DC.
TP6________________ volts DC.
TP7________________ volts DC.

m. Underline the correct response to the following statements:

(1) V_C of Q2 is equal to (0 volts, V_{CC}), and V_C of Q3 is equal to (near zero volts, V_{CC}).

(2) The malfunction that could cause both of these symptoms is that:

(a) Q2 is open
(b) Q3 is open.
(c) R4 is open.
(d) R5 is open.

LABORATORY EXERCISE

n. Consult your instructor and have him remove trouble number two and install trouble number three.

o. Leave "A" Channel probe in TP5, and use "B" Channel probe to check the amplitude of voltage at TP6 and TP7. Record these voltages below.

TP6 ________________ volts DC.

TP7 ________________ volts DC.

p. Underline the correct response to the following statements:

(1) These voltage values indicate that Q3 is (saturated, cutoff) and that the input trigger (is, is not) causing the multivibrator to switch.

(2) The malfunction that could cause the above symptoms is that:

(a) Q3 is open.

(b) Q2 is shorted.

(c) R5 is open.

(d) C3 is shorted.

q. Consult your instructor and have him remove trouble number three and insert trouble number four.

r. Leave "A" Channel probe in TP5, and use "B" Channel probe to check the voltage amplitude at TP4, TP6, and TP7. Record these values below.

TP4 ________________ volts DC.

TP6 ________________ volts DC.

TP7 ________________ volts DC.

s. Underline the correct response to the following statements:

(1) V_C of Q2 is (0 volts, high) and V_C of Q3 is (0 volts, high).

(2) The malfunction that could cause these symptoms is that:

(a) Q3 is shorted.

(b) Q3 is open.

(c) R5 is open.

(d) R4 is open.

t. Summary: Underline the correct response to the following statements:

(1) The PRT of a monostable multivibrator is the same as the input trigger PRT. (True, False)

(2) Pulse width of the monostable multivibrator used in this project is controlled by the (input trigger, value of R5 and C3).

(3) An input trigger causes Q2 to (cutoff, saturate) and Q3 to (cutoff, saturate).

(4) Capacitor C3 starts to (charge, discharge) when the trigger is applied to Q2.

(5) During the discharge of C3, Q3 is held at (cutoff, saturation).

(6) When C2 is open, Q2 remains (saturated, cutoff) and Q3 remains (saturated, cutoff).

(7) Zero volts on the collector of Q2 can be caused by an open (Q2, R4).

(8) Shorting C3 causes the forward bias on Q3 to (increase, decrease), keeping Q3 in a (cutoff, conducting) state.

(9) Shorting Q3 causes its collector voltage to be equal to 0 volts, V_{CC}).

(10) A square wave output can be taken from either or both of the (collectors, bases) of Q2 and Q3, and the signals will be (in, 180 degrees out of) phase with each other.

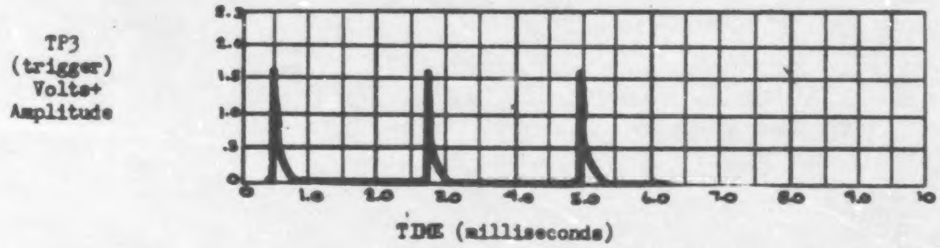
CONFIRM YOUR RESPONSES BEGINNING ON THE NEXT EVEN NUMBERED PAGE.

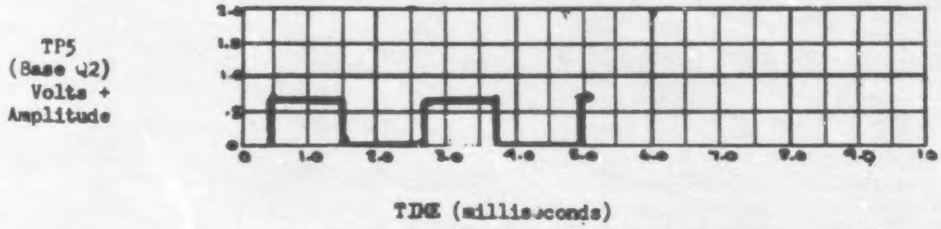
ANSWERS TO LABORATORY EXERCISE:

3. a) TP3 1.6 Vpk
   TP5 .7 Vpk

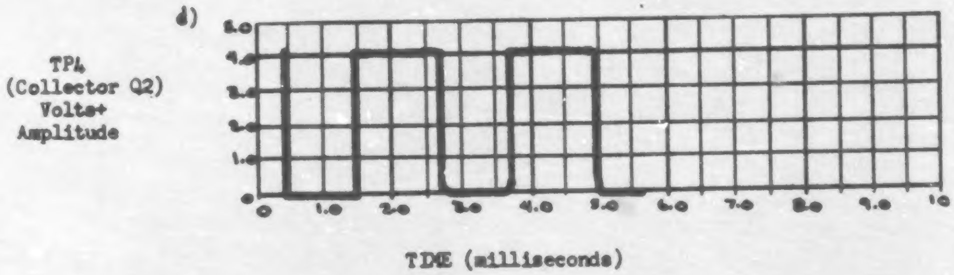
   b) PRT 2.25 milliseconds
   PRF 444 Hz

   c)



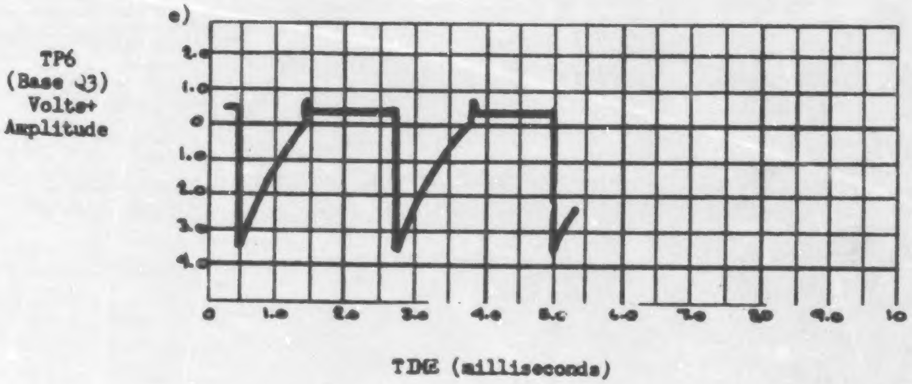


d)

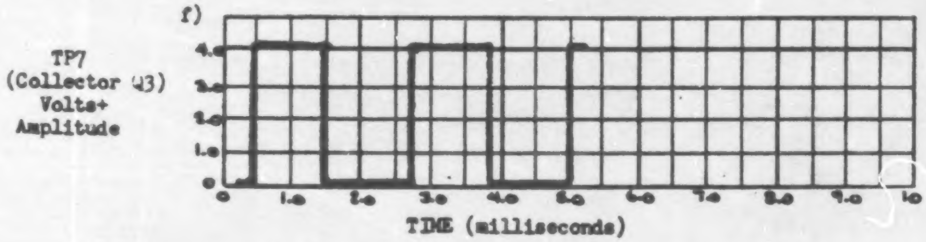


3. (continued)

e)



f)



g) 1. saturation, cutoff.
2. trigger PRT
3. the same as.
4. cutoff, saturated.
5. 180 degrees out of.
6. 180 degrees out of.
7. in.

h) Pulse width .9 milliseconds.
Rest Time 1.35 milliseconds

j) Pulse width 1.4 milliseconds.
Rest Time .8 milliseconds.

1. increased, decreased.
2. increased
3. c-R5 has increased.

LABORATORY EXERCISE

l. TP4 0 volts DC.
TP6 .6 volts DC.
TP7 .1 volts DC.

m. 1. 0 volts, near zero volts.
2. c-R4 is open.

o. TP6 .8 volts DC.
TP7 .02 volts DC.

p. 1. saturated, is not.
2. b-Q2 is shorted.

r. TP4 4 volts DC.
TP6 .6 volts DC.
TP7 0 volts DC.

s. 1. high, 0 volts.
2. Q3 is shorted.

t. 1. True.
2. Value of R5 and C3.
3. saturate, cutoff.
4. discharge.
5. cutoff.
6. cutoff, saturated.
7. R4.
8. increase, conducting.
9. 0 volts.
10. collectors, 180 degrees out of.

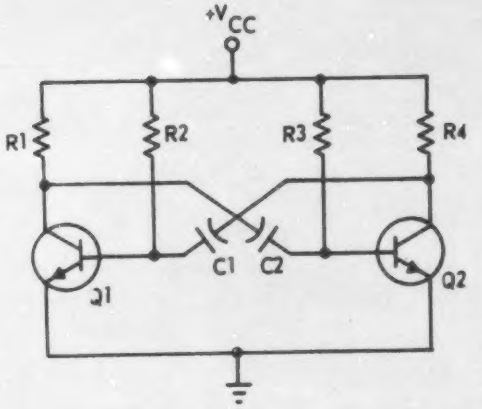
If your response to ANY of the statements is wrong, or, if ANY of your measurements are more than 10% different from those given, go back and repeat that portion of the lab project. If necessary, review the referenced text for clarification. Your instructor will assist if needed.

CONSULT YOUR INSTRUCTOR FOR CRITERION CHECK.

YOU MAY STUDY ANOTHER RESOURCE OR TAKE THE MODULE SELF-CHECK.

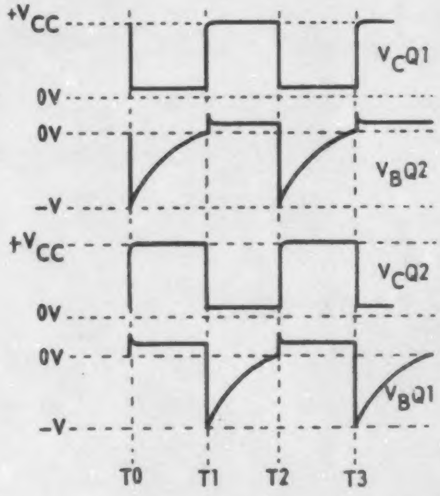
SOLID STATE MULTIVIBRATORS

Questions 1 thru 4, refer to Figure 12 and Chart 5.



REP4-1860

Figure 12



REP4-1858

Chart 9

1. The circuit in Figure 12 is correctly identified as a (triggered, free-running) (astable, monostable, bistable) multivibrator.

2. Given: The waveform labeled "A" on Chart 9 is the signal from the collector of Q2. Match the remaining waveforms to the proper element ofthe Figure 12 transistors.

Collector Q1 ______________________

Base Q1 ______________________

Base Q2 ______________________

3. Increasing the value of R2 or C1 would cause (Q1, Q2) to be cutoff longer, and (Q1, Q2) to be saturated longer.

4. Given: V_C Q1 and V_C Q2 are very low, and they remain at the same value. A possible trouble is

______ a. R2 open.

______ b. C1 open.

______ c. R3 open.

______ d. Q2 open.

MODULE SELF-CHECK

Questions 5 thru 7, refer to Figure 13 and Chart 10.

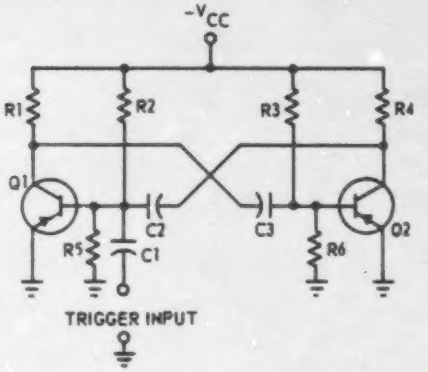

-VCC
R1
R2
R3
R4
Q1
C2
C3
Q2
R5
C1
R6
TRIGGER INPUT

Figure 13

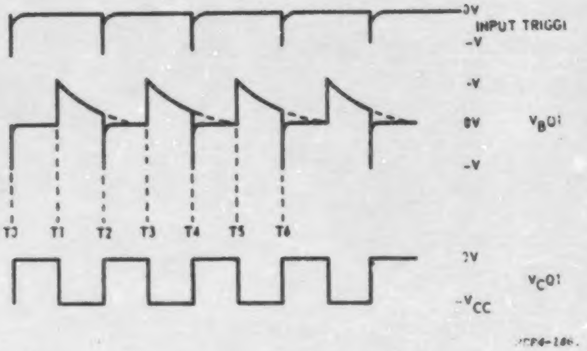


Chart 10

5. The circuit in Figure 13 is correctly identified as a (triggered, free-running) (Astable, Monostable, Bistable) multivibrator.

6. The purpose of using input triggers to this circuit is to

_______ a. increase pulse width.

_______ b. decrease pulse width.

_______ c. impair frequency stability.

_______ d. improve frequency stability.

7. On Chart 6, the time from T1 to T3 is called _______________ _______________ _______________; this time is controlled by the (trigger frequency, RC Time Constants).

Questions 8 through 12, refer to Figure 14 and Chart 11.

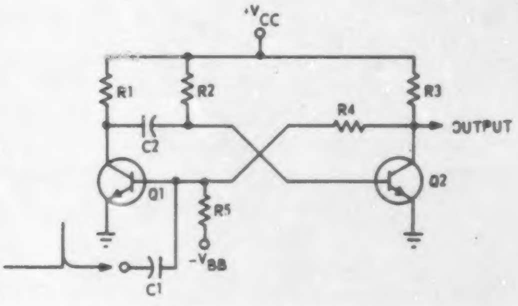

-VCC
R1
R2
R3
R4
OUTPUT
C2
Q1
Q2
R5
-VBB
C1

Figure 14

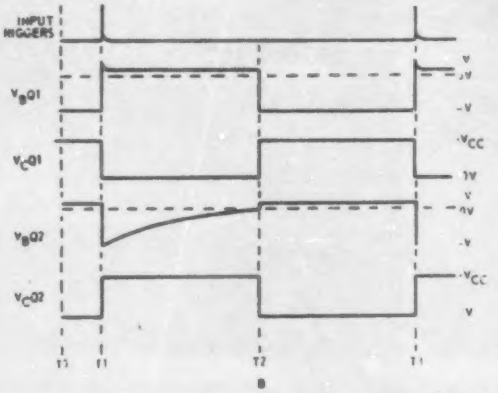


Chart 11

8. The circuit in Figure 14 is correctly identified as a (triggered astable, monostable, bistable) multivibrator.

9. Before triggers are applied, (Q1, Q2) remains cutoff and (Q1, Q2) remains saturated.

10. On Chart 11, the width of the output pulse (T1 to T2) is controlled by the

_____ a. amplitude of the input trigger.

_____ b. frequency of the input trigger.

_____ c. values of C2 and R2.

_____ d. values of C1 and R5.

11. Increasing the PRT of the input triggers would cause (an increase, a decrease, no change) in output frequency, and (an increase, a decrease, no change) in output pulse width.

12. In order to make the ouput pulse width of this circuit manually variable, it is necessary to replace

_____ a. R2 with a potentiometer.

_____ b. C1 with a variable capacitor.

_____ c. R3 with a potentiometer.

_____ d. the trigger circuit.

Questions 13 thru 18, refer to Figure 15 and Chart 12.

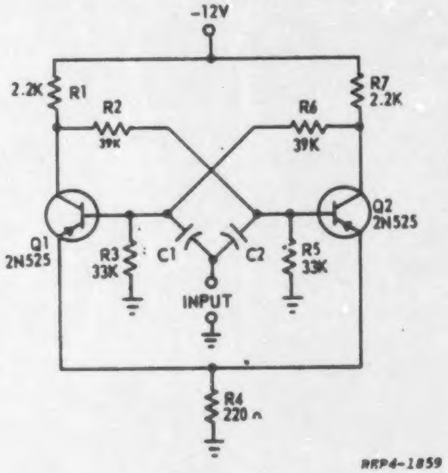


Figure 15

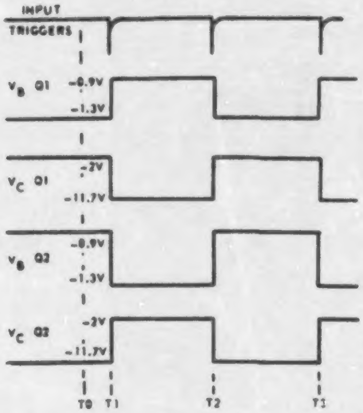


Chart 12

MODULE SELF-CHECK

13. Application of the input trigger signal to (only one, both) transistors, and a common (emitter, collector), resistor, identifies this circuit as a/an (astable, monostable, bistable) multivibrator.

14. The input trigger frequency to this circuit is (1/2, twice) the output frequency, and the input trigger PRT is (1/2, twice) the output signal PRT.

15. The input trigger frequency to this circuit controls (only the output frequency, only the output pulse width, both output frequency and output pulse width).

16. Symptom: V_C Q1 = V_{CC} Q2 = V_{CC}. A possible trouble is

______a. Q2 shorted.

______b. Q1 open.

______c. C2 shorted.

______d. R4 open.

17. Symptom: Each negative input trigger causes a positive trigger on the collector of Q1, and a negative trigger on the collector of Q2. A possible trouble is

______a. R6 open.

______b. C1 open.

______c. R2 open.

______d. C2 open.

18. Forward bias on Q2 could be reduced to 0 by an open

______a. R5.

______b. R2.

______c. R6.

______d. R3.

Questions 19 through 25, refer to Figure 16.

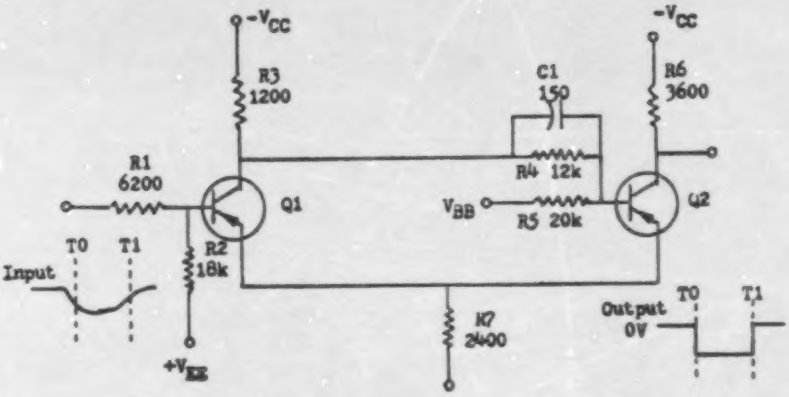


Figure 16

19. The two major purposes of the Schmitt Trigger are wave ______________ and voltage level ______________ .

20. Before the input signal is applied to the figure 16 circuit, Q1 is (cutoff, saturated) and Q2 is (cutoff, saturated).

21. At T0 of the input signal, Q1 is driven into (cutoff, saturation), and VCQ2 goes to (-VCC, 0) volts.

22. The purpose of C1 is to prevent (high, low) frequency distortion in the output signal.

23. Symptoms: VCQ1 equals -VCC; VCQ2 very nearly equals zero volts. A possible trouble is

______a. Q1 open.
______b. R1 open.
______c. C1 shorted.
______d. all of the above.

24. Symptom: VCQ2 very nearly equals VCC. A possible trouble is

______ a. R1 open.
______b. R4 open.
______c. C1 shorted.
______d. R6 open.

25. Symptom: Output signal shows high frequency distortion. A possible trouble is that

______ a. C1 is shorted.
______ b. the input signal has high frequency distortion.
______ c. C1 is open.
______d. Q2 is semi-saturated.

CONFIRM YOUR ANSWERS ON THE NEXT EVEN NUMBERED PAGE.

MODULE SELF-CHECK

ANSWERS TO MODULE SELF-CHECK.

1. free-running, astable
2. Collector Q1 C
   Base Q1 B
   Base Q2 D
3. Q1, Q2.
4. b. C1 open.
5. triggered, astable
6. d. improve frequency stability.
7. pulse recurrence time, trigger frequency
8. Monostable
9. Q1, Q2
10. c. values of C2 and R2.
11. a decrease, no change
12. a. R2 with a potentiometer.
13. both, emitter, bistable.
14. twice, 1/2
15. both output frequency and output pulse width
16. d. R4 open.
17. a. R6 open.
18. b. R2.
19. shaping, sensing.
20. cutoff, saturated.
21. saturation, -VCC.
22. high.
23. d
24. b
25. c.

HAVE YOU ANSWERED ALL OF THE QUESTIONS CORRECTLY? IF NOT, REVIEW THE MATERIAL OR STUDY ANOTHER RESOURCE UNTIL YOU CAN ANSWER ALL QUESTIONS CORRECTLY. IF YOU HAVE, CONSULT YOUR INSTRUCTOR FOR FURTHER INSTRUCTION.

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KEP-GP-48

Technical Training

Electronic Principles (Modular Self-Paced)

Module 48

SOLID STATE SAWTOOTH GENERATORS

March 1976

AIR TRAINING COMMAND

7-10

Designed For ATC Course Use

ATC Keesler 6-4168

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Electronic Principles LRC
Keesler Air Force Base, Mississippi

ATC GP 3AQR3X020-X
KEP-GP-48
March 1976

ELECTRONIC PRINCIPLES (MODULAR SELF-PACEL,

MODULE 48

SOLID STATE SAWTOOTH GENERATORS

This Guidance Package is designed to guide you through this module of the Electronic Principles Course. This Guidance Package contains specific information, including references to other resources you may study, enabling you to satisfy the learning objectives.

CONTENTS

Title	Page
Overview	1
List of Resources	1
Adjunct Guide	1
Laboratory Exercise	4
Module Self-Check	8
Answers	10

OVERVIEW

1. SCOPE: Certain applications in electronics, such as cathode ray tube deflection, require voltages that are neither square nor sinusoidal in shape. One such waveshape is the sawtooth. In this module you will learn how this signal is produced. Depth of coverage will be such that you should also be able to determine frequency and amplitude of the output signal, the methods used to produce a linear output, and logical procedures for troubleshooting.

2. OBJECTIVES: Upon completion of this module you should be able to satisfy the following objectives.

a. Given the schematic diagram of a sawtooth generator and a list of statements, select the statement that describes the effects on output linearity when time constants, applied voltage, and input gate duration are changed.

b. Given a trainer having a semiconductor sawtooth generator circuit, multimeter, and oscilloscope, measure the output amplitude and rise time within ±10 percent accuracy.

c. Given a trainer with a malfunctioning sawtooth generator circuit, a schematic diagram, multimeter, and oscilloscope, determine the faulty component two out of three times.

LIST OF RESOURCES

To satisfy the objectives of this module, you may choose, according to your training, experience, and preferences, any or all of the following.

READING MATERIALS:

Digest
Adjunct Guide with Student Text VI

Supersedes KEP-GP-48, dated December 1975.

272

AUDIOVISUALS:

Television Lesson 30-817, Unijunction Sawtooth Generator

LABORATORY EXERCISE:

Laboratory Exercise 48-1, Solid State Sawtooth Generators

AT THIS POINT, IF YOU FEEL THAT THROUGH PREVIOUS EXPERIENCE OR TRAINING YOU ARE FAMILIAR WITH THIS SUBJECT, YOU MAY TAKE THE MODULE SELF-CHECK. IF NOT, SELECT ONE OF THE RESOURCES AND BEGIN STUDY.

CONSULT YOUR INSTRUCTOR IF YOU NEED HELP.

ADJUNCT GUIDE

INSTRUCTIONS:

Study the referenced materials as directed.

Return to this guide and answer the questions.

Confirm your answers against the answers at the back of this Guidance Package.

Contact your instructor if you experience any difficulty.

Begin the program.

A. Turn to Student Text, Volume VI, and study paragraphs 6-1 through 6-9. Return to this page and answer the following statements/questions.

1. For an RC circuit to produce a linear output across the capacitor, voltage across the capacitor must not be allowed to attain a value in excess of _____ % of the applied voltage.

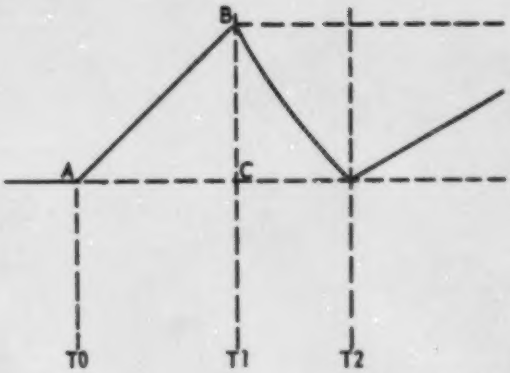

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Figure 48-1

2. Refer to figure 48-1 and match the terms in column A to the information in column B.

A	B
____(1) Linear Slope	a. B to C
____(2) Sweep Time	b. T0 to T1
____(3) PRT	c. T1 to T2
____(4) Fall Time	d. T0 to T2
____(5) Electrical Length	e. A to B
____(6) Amplitude	
____(7) Physical Length	

CONFIRM YOUR ANSWERS.

B. Turn to Student Text, Volume VI, and study paragraphs 6-10 through 6-22. Return to this page and respond to the following statements/questions.

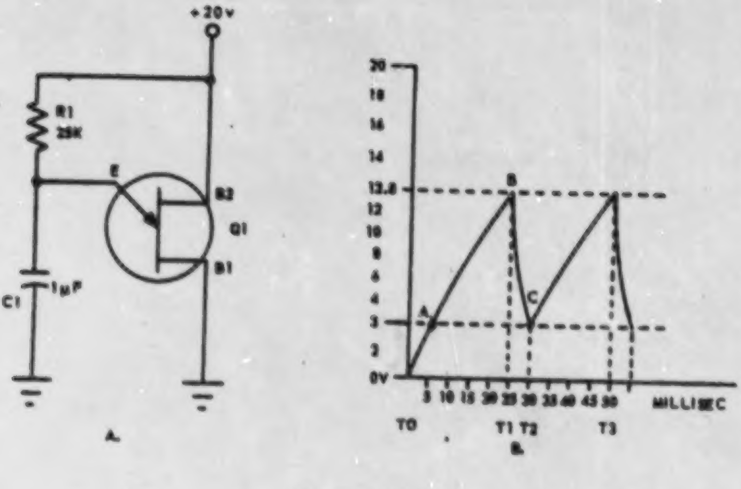

Figure 48-2

For questions 1 through 9 refer to figure 48-2 as necessary.

1. The output waveform (Part B) of the figure, 48-2, circuit could be observed on the (emitter) (Base 1) (Base 2) of the unijunction transistor.

2. The valley point of the output waveform (Part B) is represented by the letter (B) (C) and the peak point is represented by the letter (B) (C).

3. The charge path for capacitor C1 is through (R1) (Q1) to V_{CC}; its discharge path is through (R1 and V_{CC}) (Q1).

4. When C1 is charging the emitter to base (B1) resistance is (low) (high) because the unijunction transistor is (reverse) (forward) biased.

5. Linearity of the output signal from the figure 48-2 circuit could be improved by disconnecting R1 from the +20 volts and connecting it to a (higher) (lower) voltage.

6. The PRF of the output signal is _____ Hz.

7. The output waveform is (linear) (nonlinear) because C1 charges to (more) (less) than 10 percent of the applied voltage before the emitter to base (B1) junction becomes forward biased.

8. Output frequency is controlled by the value of (R1 and C1) (applied voltage), and amplitude is controlled by the value of (R1 and C1) (applied voltage).

9. In order to attain a more stable output frequency, the figure 48-2 circuit could be slightly modified and the frequency controlled by applying a negative trigger to the (emitter) (Base 2) element.

CONFIRM YOUR ANSWERS.

C. Turn to Student Text, Volume VI, and study paragraphs 6-23 through 6-37. Return to this page and answer the following statements/questions.

For questions 1 through 9 refer to figure 48-3 and figure 48-4 as necessary.

1. Before the input gate is applied to the transistor sawtooth generator (figure 48-3), Q1 is biased near (cutoff) (saturation). After the input is applied, the (positive) (negative) going portion of the input gate (saturates) (cuts off) Q1, and C1 starts to charge.

2. When the input gate goes (positive) (negative), Q1 is again (saturated) (cut off), and C1 begins to discharge.

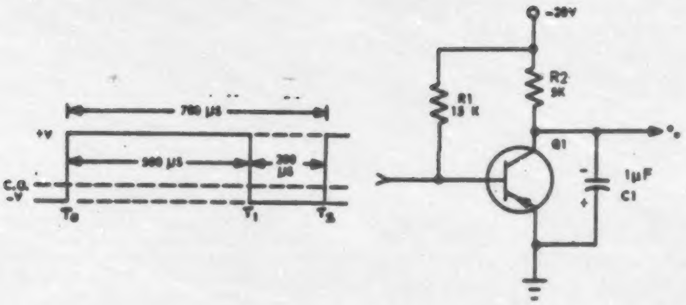

Figure 48-3

3. The output frequency is controlled by the (input signal) (size of C1 and R2).

4. Frequency of the output from the figure 48-3 sawtooth generator is ______ Hz.

5. Using the formula:

$$\% \text{ charge} = \frac{E_{Cmax} - E_{Cmin}}{V_{CC} - E_{Cmin}} \times 100$$

and information from figures 48-3 and 48-4, calculate the percentage of V_{CC} that C1 is allowed to charge.

% charge = ______%

6. The sawtooth output from figure 48-3 is (linear) (nonlinear); increasing the width of the positive going input gate (T0 to T1) would (improve) (impair) the linearity.

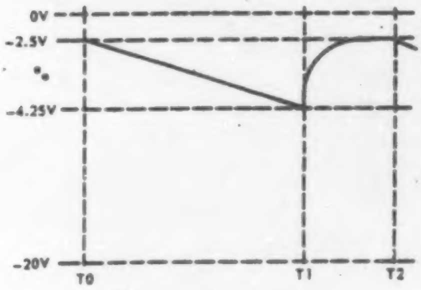

Figure 48-4

7. The output linearity from the figure 48-3 sawtooth generator could be improved by

a. replacing C1 with a larger capacitor.

b. replacing R2 with a larger resistor.

c. decreasing the width of input gate from T0 to T1.

d. all of the above.

8. An oscilloscope connected from collector to ground displays zero volts. The input gate is normal. A possible trouble is

a. R1 open.

b. Q1 open.

c. R2 shorted.

d. C1 shorted.

9. Given the information in figures 48-3 and 48-4, if the positive input gate is removed, a multimeter connected from the collector to ground would indicate approximately

a. 0 volts.

b. -4.25 volts.

c. -2.5 volts.

d. -20 volts.

CONFIRM YOUR ANSWERS.

D. Turn to Laboratory Exercise 48-1. This exercise will enable you to prove the principles of unijunction and transistor sawtooth generators. Too, you will continue to practice the use of the oscilloscope and multimeter as an aid to circuit checking and troubleshooting.

YOU MAY STUDY ANOTHER RESOURCE OR TAKE THE MODULE SELF-CHECK.

LABORATORY EXERCISE 48-1

OBJECTIVES:

1. Given a trainer having a semiconductor sawtooth generator circuit, multimeter and oscilloscope, measure the output amplitude and rise time within ±10 percent accuracy.

2. Given a trainer with a malfunctioning sawtooth generator circuit, a schematic diagram, multimeter, and oscilloscope, determine the faulty component two out of three times.

EQUIPMENT:

1. Sweep Generator Trainer (DD5932)

2. Oscilloscope

3. Multimeter

4. Transistor Circuit Power Supply (DD4885)

REFERENCE:

Student Text, Volume 6, paragraphs 6-1 through 6-29

CAUTION: OBSERVE BOTH PERSONNEL AND EQUIPMENT SAFETY RULES AT ALL TIMES. REMOVE WATCHES AND RINGS.

PROCEDURES:

1. Equipment preparation

a. Oscilloscope

Controls	Position
POWER	ON
CH1 Vertical Pos.	ON
CH2 Vertical Pos.	ON
CHOP-ALT	ALT
SEPARATE - CH1 & CH2	SEPARATE
AC-GND-DC	DC
AC-GND-DC	DC
VOLTS/CM CH1	2 CAL (change as required)
VOLTS/CM CH2	2 CAL (change as required)
TIME/CM	0.5 mS CAL
TRIG SELECT	EXT +
LEVEL	AUTO
PULL X10 MAG	Push in (normal)
FOCUS & INTENSITY	Adjust for clear presentation

b. Trainer

NOTE: You WILL NOT, at any time, open the hinged panel on the back of the trainer.

(1) S1 to R11

(2) S2 to C5

(3) S4 UP

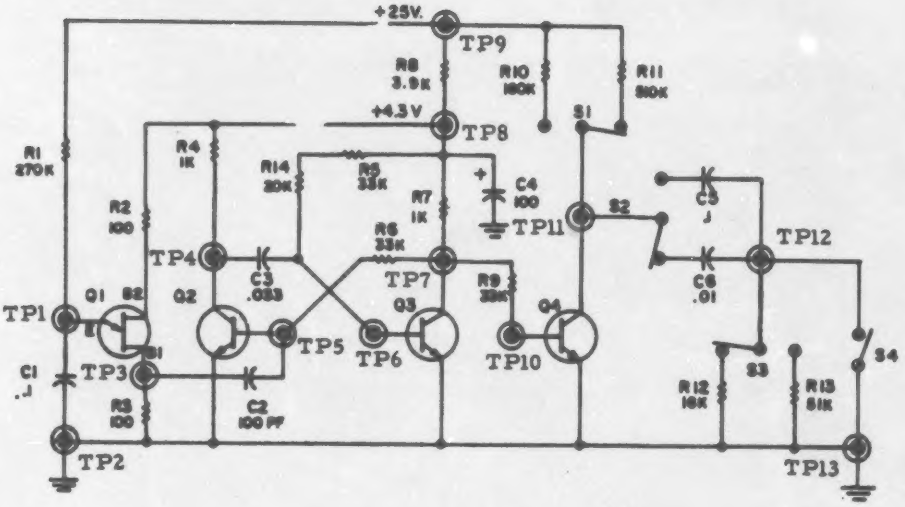
+25V.
TP9
R8
3.9K
R10
180K
R11
510K
+4.3V
TP8
S1
R1
270K
R4
1K
R14
20K
R5
33K
+
C4
100
R7
1K
C5
.1
S2
TP11
R2
100
R6
33K
TP12
TP4
C3
.033
TP7
R9
33K
C6
.01
Q1
B2
Q2
Q3
Q4
TP1
E
TP5
TP6
TP10
B1
S4
C1
.1
TP3
S3
R12
18K
R13
51K
R3
100
C2
100 PF
TP2
TP13

Figure 48-5

c. Interconnections

(1) Connect power supply to trainer with power cable.

(2) Ground oscilloscope to trainer at TP13.

(3) Connect EXT TRIG input to TP5.

d. Power Supply

(1) ON/OFF
Switch ON

(2) VOLTS ADJ Adjust for 25 volts (use built in meter).

2. Trainer Analysis (see fig. 48-5)

Q1, and its associated components comprise a unijunction trigger generator. The trigger from B1 of the unijunction transistor is used to key a monostable multivibrator (Q2 and Q3). The square wave output from the monostable multivibrator is used for gating the transistor sawtooth generator (Q4) on and off. Various combinations of resistance and capacitance can be switched into the circuit to illustrate the effect that the changing of these values have on circuit linearity, rise time (electrical length), and amplitude (physical length). Provisions are also made for simple troubleshooting.

3. Activity

NOTE: For this project, the oscilloscope is used for measuring DC voltages. Therefore, it is recommended that you review Lab Project 20-3 (Module 20) before continuing.

a. Establish 0 volts DC reference for CH1 on second line from top of oscilloscope. Establish 0 volts DC reference for CH2 on bottom line of oscilloscope.

b. Connect CH1 probe to TP3. Determine the amplitude of the signal and record below.

TP3 ________________ volts pk.

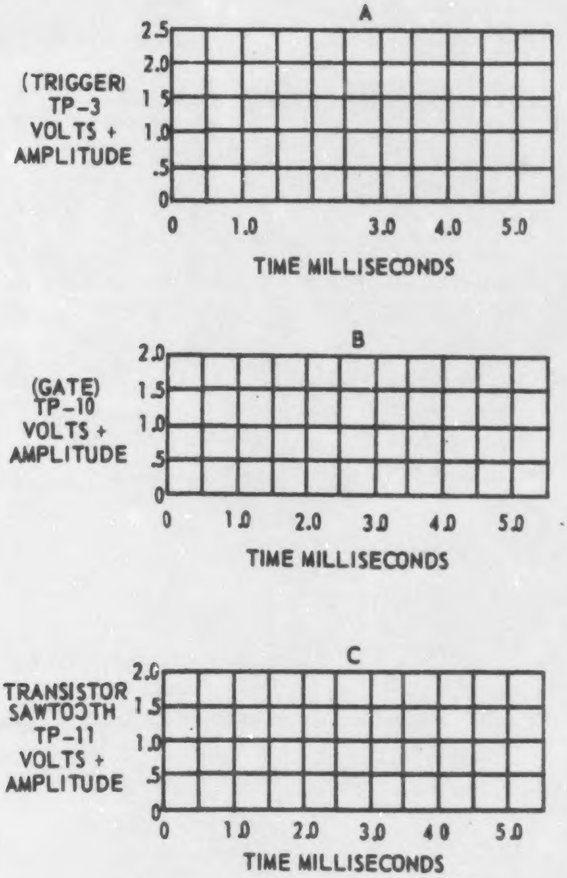

Figure 48-6

c. Draw the signal appearing at TP3 on figure 48-6A.

d. Leaving CH1 probe in TP3, connect CH2 probe to TP10. Draw the signal appearing at TP10 on figure 48-6B.

e. Move CH2 probe to TP11; draw this signal on figure 48-6C.

f. Underline the correct response to the following statements:

(1) The PRT of the output signal from the transistor sawtooth generator (TP11) is (longer than) (shorter than) (the same as) the PRT of the unijunction trigger generator (TP3).

(2) The rise time of the transistor sawtooth signal is determined by the width of the (positive going) (negative going) gate at TP10.

(3) In order for a sawtooth signal to be developed at TP11, Q4 must be (saturated) (cut off) by the incoming signal, allowing C5 to (charge) (discharge) through (R11) (Q4).

(4) The signal at TP11 is (linear) (nonlinear) because the capacitor charged to (more) (less) than 10 percent of V_{CC}.

(5) The time constant of C5 and R11 is (long) (short), causing C5 to charge (rapidly) (slowly) during the time Q4 is cut off.

g. Refer to figure 48-6 and determine the value of the following sawtooth terms.

(1) Rise time or Sweep time ________ ms

(2) Amplitude ________ volts

(3) PRT ________ ms

h. Change S1 to the R10 position, and S2 to the C6 position. Using CH2 probe, measure the amplitude, PRT, and sweep time of the signal at TP11, and record in the spaces below. Set Volts/CM CH2 to 5V.

Amplitude ________ volts

PRT ______ milliseconds.

Sweep time ______ milliseconds.

i. Underline the correct response to the following statements:

(1) R10 is (more) (less) than R11, and C6 is (more) (less) than C5, causing a (longer) (shorter) time constant.

(2) The sawtooth signal at TP11 is (linear) (nonlinear) because C6 is charging to (more) (less) than 10 percent of V_{CC}.

(3) Changing the RC time constant caused (an increase) (a decrease) (no change) in amplitude.

j. Return S1 to R11 and S2 to C5. Consult your instructor and have him insert trouble number 1 (S9).

k. Leaving CH1 probe in TP3, use CH2 probe to recheck the signals at TP10 and TP11. Compare the signals observed to those recorded in figure 48-6. Underline the correct response to the following statements.

(1) The signal appearing at (TP10) (TP11) shows very little change, while the voltage at (TP10) (TP11) has (increased) (decreased) greatly.

(2) These values indicate that

______ (a) Q4 is shorted.
______ (b) Q4 is open.
______ (c) R11 is open.
______ (d) C5 is shorted.

l. Consult your instructor, and have him remove trouble number one and insert trouble number 2 (S11).

m. Leaving CH1 probe in TP3, use CH2 probe to recheck the signals at TP10 and TP11. Compare the signals to those recorded in figure 48-6. Underline the correct response to the following statements. Reset CH2 Volts/CM switch as required.

(1) The signal appearing at (TP10) (TP11) shows very little change, while the voltage at (TP10) (TP11) has (increased) (decreased) to (0 volts) (nearly V_{CC}).

(2) These values indicate that

______ (a) Q4 is open.
______ (b) R11 is shorted.
______ (c) C5 is open.
______ (d) C5 is shorted.

n. Consult your instructor and have him remove trouble number two and insert trouble number three (S8).

o. Leave CH1 connected to TP3 and use CH2 to recheck the signals at TP10 and TP11. Reset CH2 VOLTS/CM switch as required. Compare the signals with those recorded on figure 48-6. Complete the following statements:

(1) The signal appearing at (TP10) (TP11) decreased to zero and the voltage at (TP10) (TP11) increased greatly.

(2) These valuse indicate that

______ (a) Q4 is open
______ (b) C5 is shorted
______ (c) R11 is open
______ (d) Q3 is shorted

p. Summary: Underline the correct response to the following statements.

(1) The (negative) (positive) going output from Q3 causes Q4 to cut off.

(2) During the time that Q4 is (saturated) (cut off), C5 charges through R11.

(3) The length of time that C5 is allowed to charge is determined by the (amplitude) (width) of the input gate.

(4) Increasing the width of the input gate would cause electrical length and physical length to (increase) (decrease), and linearity to be (improved) (impaired).

(5) The amplitude of the transistor sawtooth was (increased) (decreased) when the values of resistance and capacitance were decreased, because the capacitor charged (more) (less) while Q4 was (cut off) (saturated).

(6) Decreasing the values of resistance and capacitance associated with the transistor sawtooth generator caused linearity to be (improved) (impaired), because the RC time constant was (increased) (decreased) allowing the capacitor to charge to (more) (less) than 10 percent of V_{CC}.

(7) An open collector load causes the voltage across the transistor to be equal to (V_{CC}) (0 volts).

(8) Shorting the capacitor associated with a transistor sawtooth generator causes the output voltage to be equal to (V_{CC}) (0 volts).

CONFIRM YOUR RESPONSES ON THE BACK PAGES.

CONSULT YOUR INSTRUCTOR FOR THE PROGRESS CHECK.

MODULE SELF-CHECK

Questions 1 through 14 refer to figure 48-7.

Match the following terms (phrases) to the letters in figure 48-7B.

Terms

___1. Sawtooth Amplitude

___2. Peak

___3. Fall Time

___4. PRT

___5. Valley

___6. Physical Length

___7. C1 Discharge Time

___8. Slope

___9. Rise Time

___10. Electrical Length

Letters on Figure 48-7B

a. A to B

b. C to D

c. G

d. H

e. E to F

f. A to D

11. The circuit in figure 48-7A is correctly identified as a __________ ___________ generator.

12. C1 is (charging) (discharging) while the emitter to B1 junction is reverse biased, and is (charging) (discharging) when the emitter to B1 junction becomes forward biased.

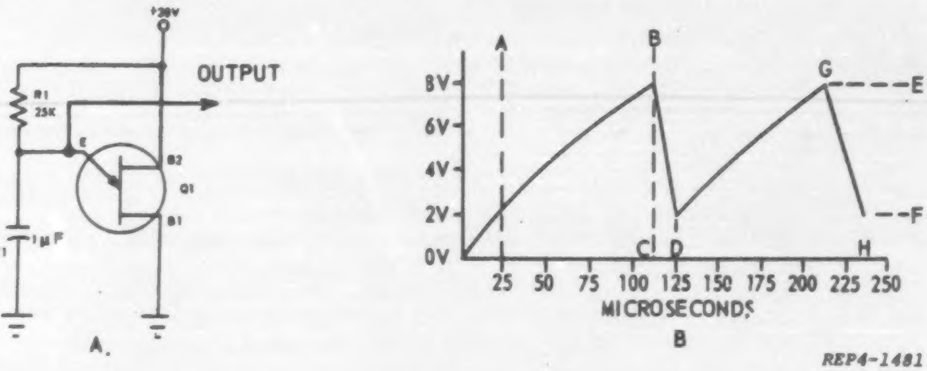

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Figure 48-7

(Given: The sawtooth wave shown in figure 48-7 is the output from the circuit.)

13. The circuit is producing a (linear) (nonlinear) sawtooth, because the capacitor charges to (more than) (less than) 10 percent of the applied voltage.

14. A method of improving linearity of the sawtooth output is to return R1 to a (higher) (lower) positive voltage than is applied to B2.

Questions 15 through 17 refer to figure 48-8.

(Given: Figure 48-8B represents the output signal from the circuit.)

15. A sawtooth output signal is produced when the (positive) (negative) going input gate causes Q1 to (cut off) (saturate).

16. Amplitude of the sawtooth signal is (500 microseconds) (1.75 volts) and the rise time is (500 microseconds) (1.75 volts).

17. Decreasing the width of the positive going input gate will cause:

a. physical length to increase.

b. electrical length to increase.

c. a decrease in linearity.

d. an improvement in linearity.

CONFIRM YOUR ANSWERS.

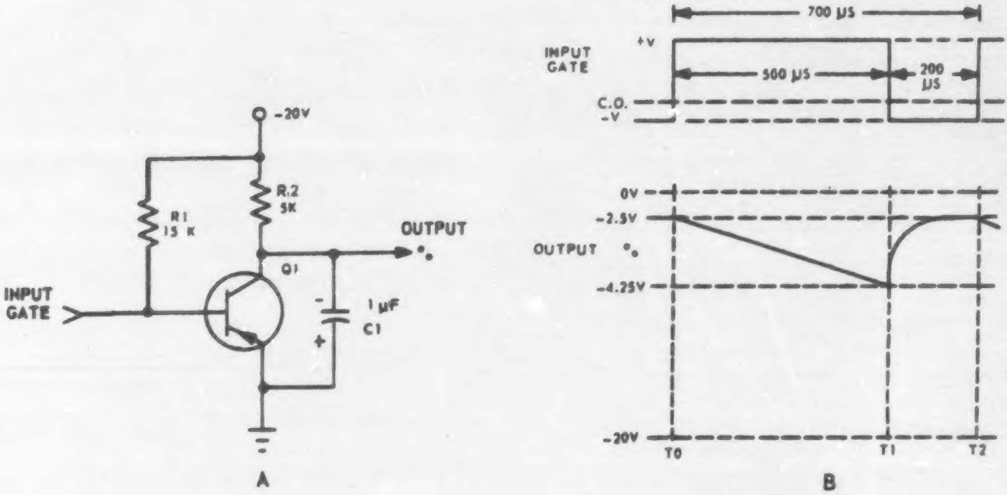
-20V
R.2
5K
R1
15 K
OUTPUT
e_o
Q1
INPUT GATE
1 µF
C1
A
700 µS
+V
INPUT GATE
500 µS
200 µS
C.O.
-V
0V
-2.5V
OUTPUT e_o
-4.25V
-20V
T0
T1
T2
B

Figure 48-8

ANSWERS TO A:

1. 10 percent
2. (1) e
   (2) b
   (3) d
   (4) c
   (5) b
   (6) a
   (7) a

If you missed ANY questions, review the material before you continue.

ANSWERS TO B:

1. emitter
2. C, B
3. R1, Q1
4. high, reverse
5. higher
6. 40 Hz
7. nonlinear, more
8. R1 and C1, applied voltage
9. Base 2

If you missed ANY questions, review the material before you continue.

ANSWERS TO C:

1. saturation, positive, cuts off
2. negative, saturated
3. input signal
4. 1,428 Hz
5. 10 percent
6. linear, impair
7. d
8. d
9. c

If you missed ANY questions, review the material before you continue.

ANSWERS TO LABORATORY EXERCISE:

3.

b. TP3 1.7 volts pk.

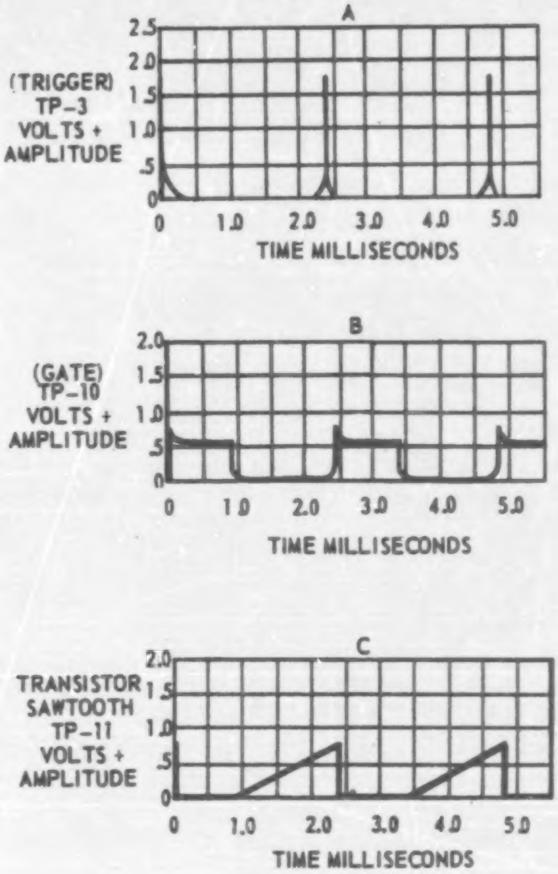

Figure 48-6

f. (1) the same as
   (2) 1.3, negative going
   (3) cut off, charge, R11
   (4) linear, less
   (5) long, slowly

g. (1) Rise time - 1.3 ms
   (2) Electrical length - 1.3 ms
   (3) Physical length - 0.6 volt DC
   (4) PRT - 2.25 ms

h. Amplitude - 12 volts pk
   PRT - 2.25 ms
   Sweep time - 1.3 ms

i. (1) less, less, shorter
   (2) nonlinear, more
   (3) an increase

k. (1) TP10, TP11, increased
   (2) (b) Q4 is open.

m. (1) TP10, TP11, decreased, 0 volts.
   (2) (d) C5 is shorted.

o. (1) TP10, TP11
   (2) (d) Q3 is shorted.

p[illegible] (1) negative

(2) cut off

(3) width

(4) increase, impaired

(5) increased, more, cut off

(6) impaired, decreased, more

(7) 0 volts

(8) 0 volts

If your response to ANY of the statements is wrong, or if ANY of your measurements are more than 10 percent different, go back and repeat that portion of the project. If necessary, review the referenced text material for clarification. Your instructor will assist if needed.

ANSWERS TO MODULE SELF-CHECK:

1. e
2. c
3. b
4. f
5. d
6. e
7. b
8. a
9. a
10. a
11. unijunction sawtooth
12. charging, discharging
13. nonlinear, more than
14. higher
15. positive, cut off
16. 1.75 volts, 500 microseconds
17. d

HAVE YOU ANSWERED ALL OF THE QUESTIONS CORRECTLY? IF NOT, REVIEW THE MATERIAL UNTIL YOU CAN ANSWER ALL QUESTIONS CORRECTLY. IF YOU HAVE, CONSULT YOUR INSTRUCTOR FOR FURTHER INSTRUCTIONS.

ATC GP 3AQR3X020-X
Prepared by Keesler TTC
KEP-GP-49

Technical Training

Electronic Principles (Modular Self-Paced)
Module 49

SOLID STATE TRAPEZOIDAL GENERATORS

1 September 1975

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Radar Principles Branch
Keesler Air Force Base, Mississippi

ATC GP 3AQR3X020-X
KEP-GP-49
1 September 1975

ELECTRONIC PRINCIPLES

MODULE 49

This Guidance Package is designed to guide you through this module of the Electronic Principles Course. This Guidance Package contains specific information, including references to other resources you may study, enabling you to satisfy the learning objectives.

CONTENTS

TITLE	PAGE
Overview	1
List of Resources	1
Adjunct Guide	1
Laboratory Exercise	3
Module Self-Check	8
Answers	10

OVERVIEW

1. SCOPE: There is very little difference in the Trapezoidal Generator and the Sawtooth Generator you have just finished. The trapezoidal wave is required for linear deflection of the electron beam of an electromagnetic cathode ray tube. You will learn how this type of signal is generated, the actions that can be taken to ensure a linear output signal, and basic troubleshooting techniques. The laboratory exercise will reinforce the theories discussed.

2. OBJECTIVES: Upon completion of this module you should be able to satisfy the following objectives:

a. Given the schematic diagram of a trapezoidal wave generator and a list of statements, select the statement that describes the effects on output linearity when time constants, applied voltage, and input gate duration are changed.

b. Given a trainer having a semiconductor trapezoidal wave generator circuit, multimeter, and oscilloscope, measure the output amplitude, rise time, and jump voltage within ±10 percent accuracy.

c. Given a trainer with a malfunctioning trapezoidal wave generator circuit, a schematic diagram, multimeter, and oscilloscope, determine the faulty component, two out of three times.

LIST OF RESOURCES

To satisfy the objectives of this module, you may choose, according to your training, experience, and preferences, any or all of the following:

READING MATERIALS:

Digest
Programmed Text
Adjunct Guide with Student Text VI

LABORATORY EXERCISE:

Laboratory Exercise 49-1, Solid State Trapezoidal Generator.

Supersedes KEP-GP-49, 1 May 1974. Present supplies will be used.

AT THIS POINT, IF YOU FEEL THAT THROUGH PREVIOUS EXPERIENCE OR TRAINING YOU ARE FAMILIAR WITH THIS SUBJECT, YOU MAY TAKE THE MODULE SELF-CHECK.

CONSULT YOUR INSTRUCTOR IF YOU NEED HELP.

ADJUNCT GUIDE

INSTRUCTIONS:

Study the referenced materials as directed.

Return to this guide and answer the questions.

Check your answers against the answers at the back of this Guidance Package.

Contact your instructor if you experience any difficulty.

Begin the Program.

A. Turn to Student Text, Volume VI, and study paragraphs 6-38 through 6-57. Return to this page and respond to the following statements/questions.

1. A trapezoidal voltage waveform is required for the deflection (coils)(plates) of a cathode ray tube employing (electrostatic)(electromagnetic) fields to position the electron beam.

2. Given the information on figure 49-1, match the terms in column "A" to the information in column "B".

A	B
(1) PRT . ______	a. T0 to T1
(2) Amplitude ______	b. T1 to T2
(3) Electrical Length ______	c. T0 to T3
(4) Jump Voltage ______	d. A to B
(5) Physical Length ______	e. B to C
(6) Linear Slope ______	f. C to D
(7) Fall Time ____	
(8) Sweep Time ___	

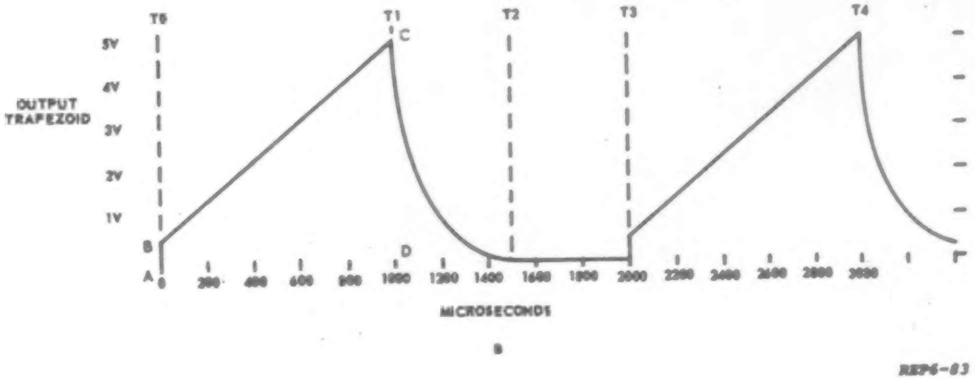
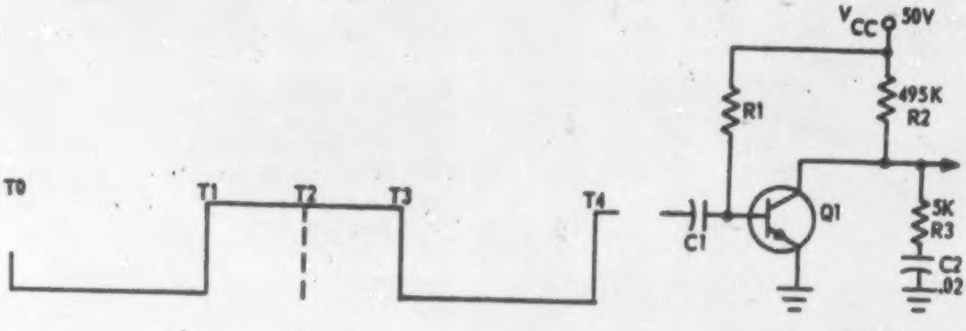


Figure 49-1. Trapezoidal Wave



REP4-1531

Figure 49-2. Trapezoidal Generator

For questions 3 through 10, refer to figures 49-1 and 49-2.

3. At T0 of the input gate Q1 goes from (saturation) (cutoff) to (saturation) (cutoff); the (sawtooth) (jump) voltage appears at the output, and C2 begins to (charge) (discharge).

4. The electrical length of the output from the circuit is determined by the (width of the negative going input gate) (width of the positive going input gate) (values of R2, R3, and C2).

5. Amplitude of the jump voltage is determined by the

______ a. value of R3 only.

______ b. value of R2 only.

______ c. value of V_{CC} only.

______ d. relative value of R2 and R3, and the amount of V_{CC}.

6. Output frequency is determined by the (input signal) (values of C2 and R3).

7. Output linearity could be improved by

______ a. decreasing the value of C2.

______ b. decreasing the width of the negative going input gate.

______ c. decreasing the value of R2.

______ d. decreasing V_{CC}.

8. An oscilloscope connected between collector and ground indicates a straight line very nearly equal to zero volts. A possible cause is

______ a. R1 open.

______ b. R3 open.

______ c. C1 open.

______ d. C2 open.

9. An oscilloscope connected between collector and ground displays a square wave that is 180 degrees out of phase with the input gate. A possible cause of this malfunction is

______ a. R3 open.

______ b. R3 shorted.

______ c. R1 open.

______ d. R1 shorted.

10. Increasing the width of the negative going portion of the input signal would cause the amplitude of the trapezoidal wave to (increase) (decrease), and the slope linearity would be (improved) (impaired).

CONFIRM YOUR ANSWERS.

B. Turn to Laboratory Exercise 49-1. This project will allow you to prove most of the principles you have learned about trapezoidal sweep generators. Also, you will continue adding to your knowledge of the oscilloscope and multimeter used in locating faulty circuit components.

YOU MAY STUDY ANOTHER RESOURCE OR TAKE THE MODULE SELF-CHECK.

LABORATORY EXERCISE 49-1

OBJECTIVES:

1. Given a trainer having a semiconductor trapezoidal wave generator circuit, multimeter, and oscilloscope, measure the output amplitude, rise time, and jump voltage within ±10 percent accuracy.

2. Given a trainer with a malfunctioning trapezoidal wave generator circuit, a schematic diagram, multimeter, and oscilloscope, determine the faulty component two out of three times.

EQUIPMENT:

1. Sweep Generator Trainer (DD-5932)
2. Oscilloscope
3. Transistor Power Supply (DD-4835)
4. Multimeter

REFERENCE:

Student Text, Volume IV, paragraphs 6-44 thru 6-57.

CAUTION: OBSERVE BOTH PERSONNEL AND EQUIPMENT SAFETY RULES AT ALL TIMES. REMOVE WATCHES AND RINGS.

PROCEDURES:

1. Trainer Analysis

For this project, the trainer will be the same as for Lab Project 48-1, except that S-4 is opened, changing the trainer from a Sawtooth Generator to a Trapezoidal Generator.

2. Equipment Preparation

a. Oscilloscope

Controls	Position
(1) Power	ON
(2) MODE	Alternate
(3) VOLTS/DIV	"A" Channel .5 Calibrated (change as required) "B" Channel 1 Calibrated (change as required)
(4) POLARITY	Normal, DC (both channels)
(5) TIME/DIV	.5 mSec, calibrated (change as required)
(6) TRIGGER SELECTOR	Auto, Ext, +

b. Interconnections

1. Ground Oscilloscope to trainer at TP13.

2. Connect Trigger input of Oscilloscope to TP1.

3. Connect Power Supply to trainer.

c. Trainer

(NOTE: You WILL NOT, at any time, open the hinged panel on back of the trainer).

(1) S1 to R11.

(2) S2 to C5.

(3) S3 to R12.

(4) S4 Down

d. Transistor Power Supply

(1) ON/OFF Switch - ON

(2) Adjust voltage to 25 volts. (Use built-in meter).

Consult your instructor and let him ensure that the trainer is in its normal operating condition.

3. Activity

(NOTE: The oscilloscope will be used for measuring DC voltage in this project. It is recommended that you review Lab Project 20-3, Module 20, before continuing.)

a. Establish 0 volts DC reference for "A" channel on the second line from the top of the oscilloscope, and 0 volts DC reference for "B" channel on the bottom line of the oscilloscope.

b. Connect "A" channel probe to TP10, and "B" channel probe to TP11. Read the following values, and record them in the space provided.

Amplitude TP10________________ volts pk.

Pulse Width
(Neg.) TP 10________________ milliseconds.

Rest Time
(Pos.) TP10________________ milliseconds.

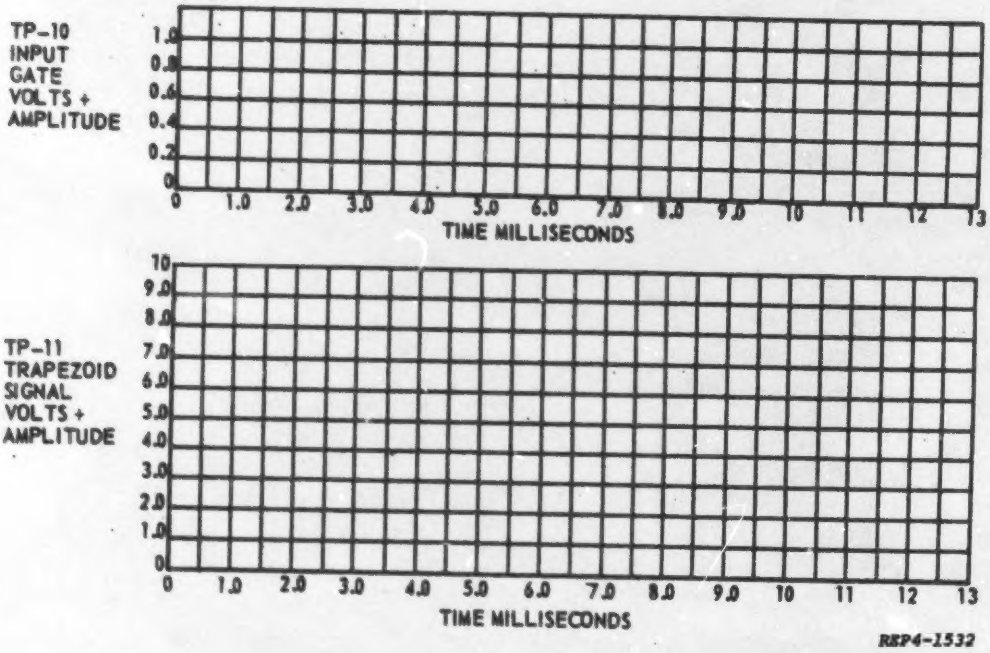
Pulse Recurrent Time
(PRT) TP10________________ milliseconds.

Amplitude TP11________________ volts pk.

Jump Voltage
TP11________________________ volts.

Rise Time TP 11________________ milliseconds.

PRT TP11__________________ milliseconds.



Graph 1

c. Draw the signals appearing at TP-10 and TP-11 on graphs provided. (NOTE: Start the positive going signal of TP-10 on the 1 msec line of Graph 1.)

d. Underline the correct response to the following statements:

(1) In order for a trapezoidal wave to be produced at TP11, Q4 must be (cutoff, saturated) by the (negative, positive) going signal from Q3.

(2) The jump voltage which changes the circuit from a sawtooth wave generator to a trapezoidal wave generator was caused by adding R12 in (series, parallel) with C5 and R11.

e. Change S3 to the R13 position. Read the amplitude of the jump voltage and slope time at TP11 and record in the space below. Underline the correct response to the statements which follow.

Jump Voltage ____________________ volts

Slope Time ____________________ milliseconds.

(1) The jump voltage amplitude (increased, decreased) because R13 is (larger, smaller) than R12.

(2) The slope time (increased, decreased, did not change).

f. Change S2 to the C6 position. Read the amplitude of the signal and slope time at TP11, and record in the space below. Underline the correct response to the statements which follow.

Amplitude ____________________ volts.

Slope Time ____________________ milliseconds.

(1) The signal amplitude (increased, decreased, did not change).

(2) The slope time (increased, decreased, did not change).

(3) Linearity was (improved, impaired) because C6 is smaller than C5, and charged to (more, less) than 10% of V_{CC}.

g. Change S2 to the C5 position and S3 to the R12 position. Consule your instructor and ask him to insert trouble number 1 (S-12).

h. Leave "A" channel probe in TP10. Using "B" channel probe, check the amplitude of the signal at TP11. Record the amplitude of both signals in the following spaces. Draw the signals on Graph 2.

Amplitude TP10____________________ volts.

Amplitude TP11____________________ volts.

i. Turn the transistor power supply ON/OFF switch to the OFF position. Using the ohmmeter, check the resistance between TP12 and ground. Record the results.

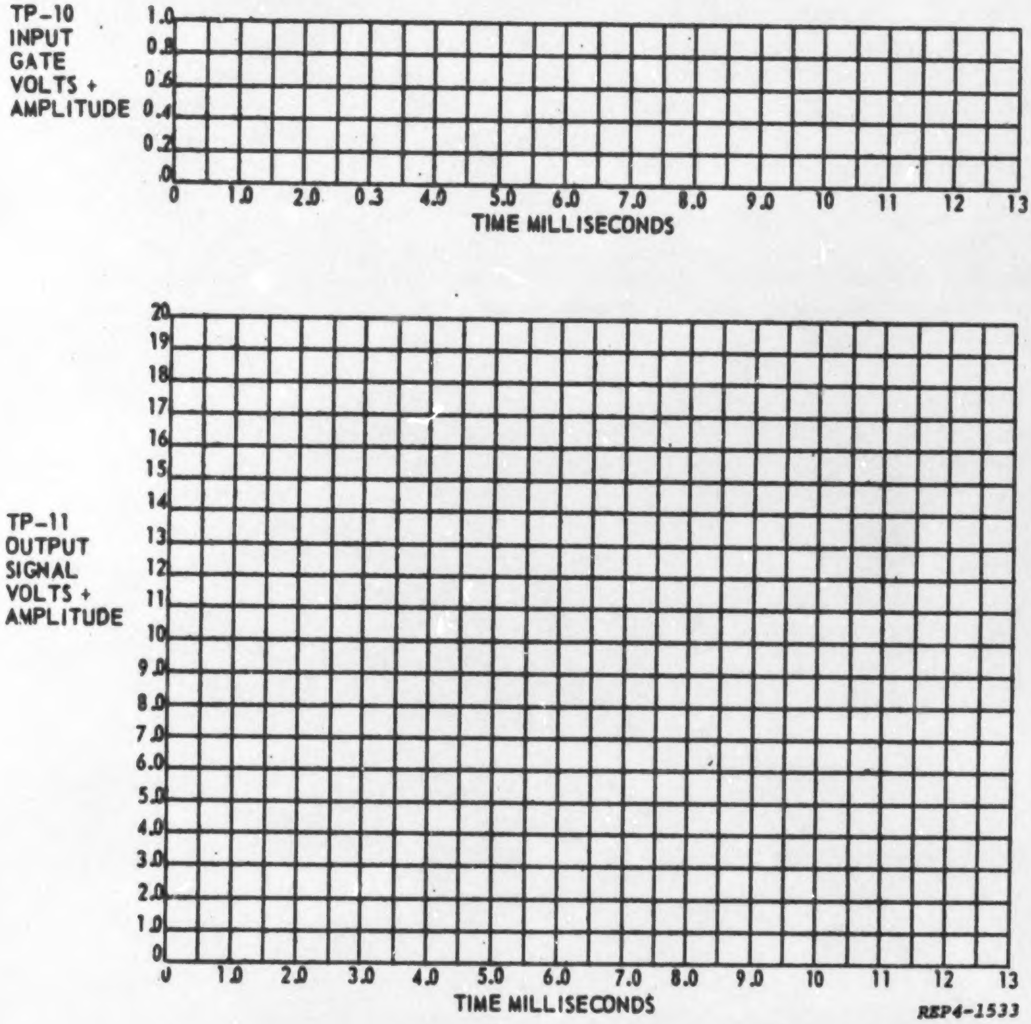
Resistance TP12____________________ Ohms.

j. Remove the ohmmeter. Turn the Transistor Power Supply ON/OFF switch to the ON position. Underline the correct response to the following statements:

(1) Q4 is now acting as a (sawtooth generator, trapezoidal generator, common emitter amplifier).

(2) All of the symptoms noted above could be caused by

(a) R12 shorted.
(b) R12 open.
(c) Q4 open.
(d) Q4 shorted.



Graph 2

k. Consult your instructor and ask him to remove trouble number 1 and insert trouble number 2 (S-8).

l. Observing the oscilloscope presentations, (TP10) on "A" channel and TP11 on "B" channel) underline the correct response to the following statements:

(1) The amplitude of the signal at TP10 has (increased, decreased to 0), and the voltage at TP11 is a (trapezoidal wave, DC voltage).

(2) These symptoms could be caused by R9 (open, shorted) or Q3 (open, shorted).

m. Consult your instructor and ask him to remove all malfunctions from the trainer.

n. Summary: Underline the correct response to the following statements:

(1) The jump voltage of a trapezoidal wave generator occurs at the first instant the transistor is (cutoff, saturated).

(NOTE: Refer to the schematic diagram on the trainer while responding to the following statements.)

(2) The amplitude of the jump voltage can be increased by increasing (R12, R11) or decreasing (R12, R11).

(3) Decreasing the capacitance of C5 causes the physical length of the output signal to (increase, decrease) and linearity to be (improved, impaired).

(4) Shorting Q3 (does, does not) disable the trapezoidal generator, because Q4 (does, does not) require an input gate in order to furnish the desired output.

(5) Opening R12 causes a/an (increase, decrease) in the voltage measured at TP11, and the resistance from TP12 to ground (increases, decreases) to (infinity, 0 Ohms).

CONFIRM YOUR RESPONSES ON THE BACK PAGES.

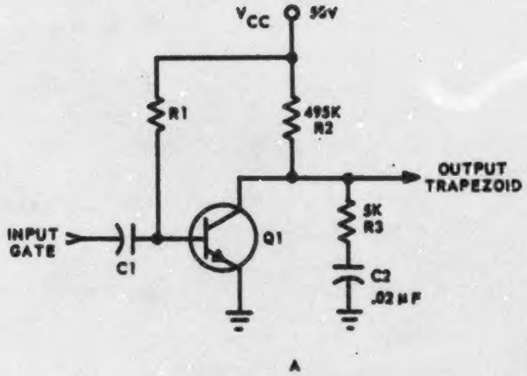

VCC
50V
R1
495K
R2
OUTPUT
TRAPEZOID
5K
R3
INPUT
GATE
C1
Q1
C2
.02 µF
A

Figure 49-3

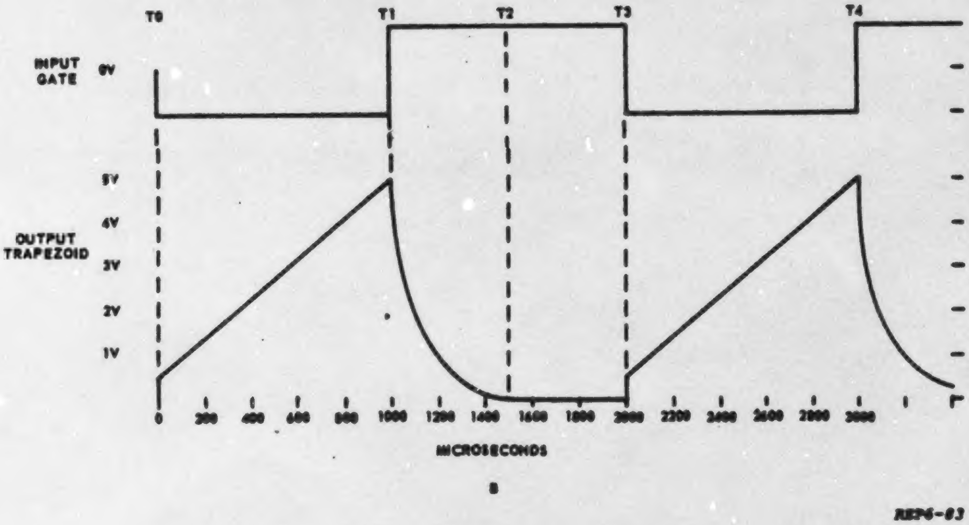


Figure 49-4

MODULE SELF-CHECK

Questions 1 thru 6 refer to figures 49-3 and 49-4.

Given: The waveshapes on figure 49-4 represent the input to (square wave) and output from (trapezoidal wave) the circuit in figure 49-3.

1. At T0, the negative going gate causes Q1 to (saturate, cutoff) and the (jump, slope) voltage occurs.

2. The amplitude of the jump voltage is approximately (1/2, 5) volts, and the amplitude of the trapezoidal wave is (1/2, 5) volts.

3. The slope time (electrical length) of the trapezoidal wave is (1, 2) milliseconds, and the signal PRT is (1, 2) millisecond.

4. Amplitude of the jump voltage is determined by the:

_____ a. input gate width.

_____ b. input gate frequency.

_____ c. value of C2 and R3.

_____ d. value of R2, R3, and V_{CC}.

5. Fall time of the trapezoidal wave is (greater, less) than the electrical length because the discharging of C2 through (Q1 and R3, R2 and R3) takes less time than the charging of C2 through (Q1 and R3, R2 and R3).

6. Increasing the gate width of the input signal would cause the electrical length of the output signal to (increase, decrease), the physical length to (increase, decrease), and the slope linearity to be (improved, impaired).

CONFIRM YOUR ANSWERS ON THE BACK PAGES.

ANSWERS TO A - ADJUNCT GUIDE:

1. coils, electromagnetic
2. (1) c (2) f (3) a (4) d (5) f (6) e (7) b (8) a
3. saturation, cutoff, jump, charge
4. width of the negative going input gate
5. d
6. input signal
7. b
8. c
9. a
10. increase, impaired.

If you missed ANY questions, review the material before you continue.

ANSWERS TO LABORATORY EXERCISE 49-1

3b. Amplitude TP10 .6 volts pk

Pulse Width (Neg) TP10 1.3 milliseconds.

Rest Time (Pos) TP10 .9 milliseconds.

PRT TP10 2.2 milliseconds.

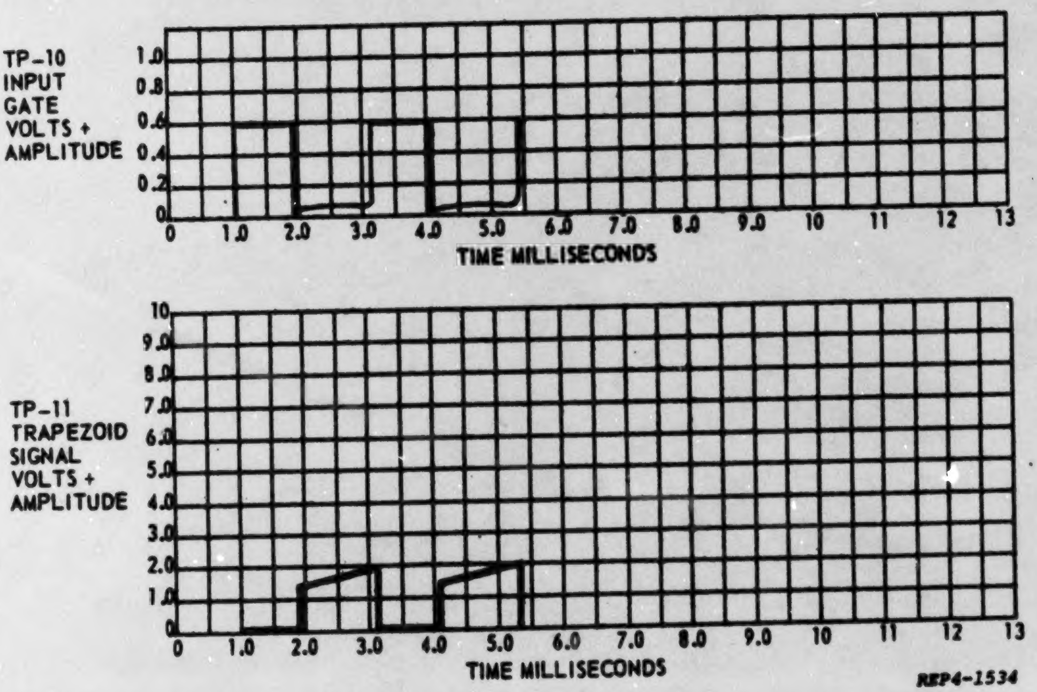
Amplitude TP11 2 volts pk.

Jump Voltage TP11 1.6 volts.

Rise Time TP11 1.3 milliseconds.

PRT TP11 2.2 milliseconds.

3c.



Graph 1

3d. (1) Cutoff, negative (2) series

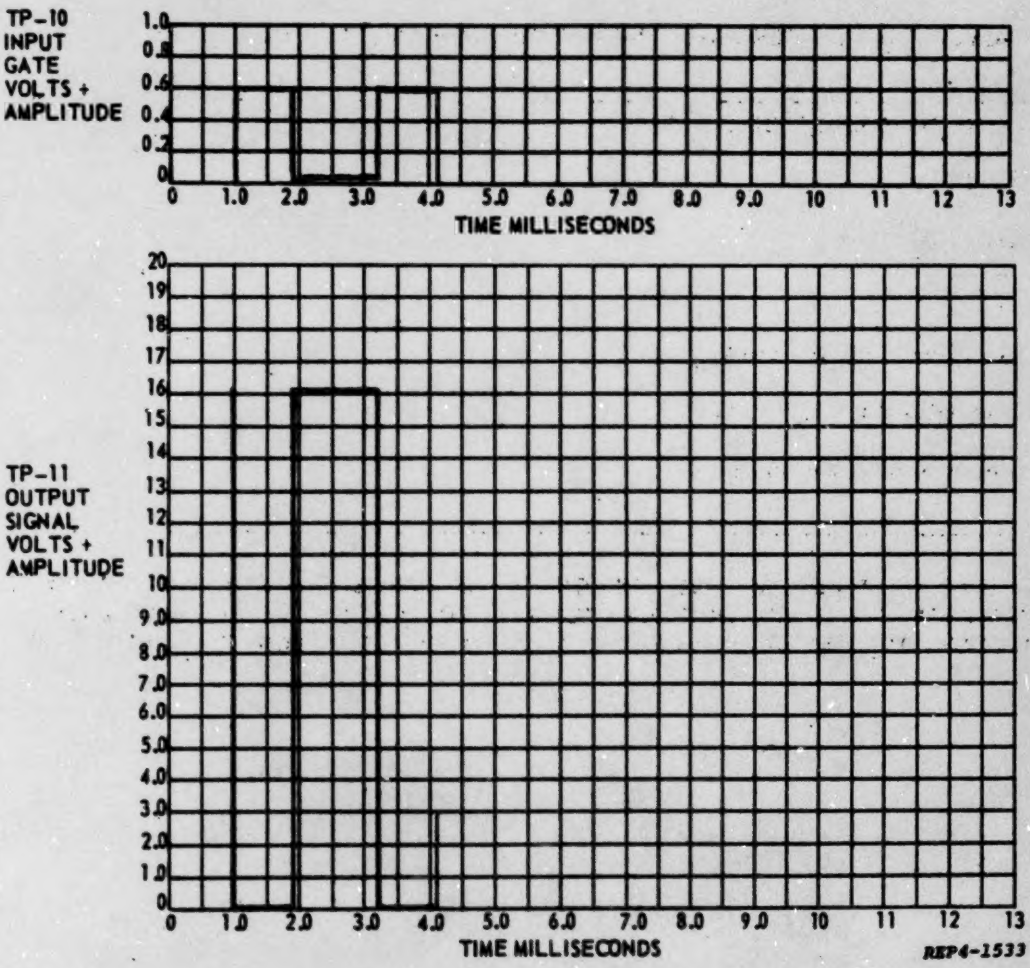
3e. Jump Voltage 4 volts. Slope Time 1.3 milliseconds.

3e (1) increased, large (2) increased (3) did not change

3f Amplitude 6.4 volts Slope Time 1.3 milliseconds.

3f (1) increased (2) did not change (3) impaired, more

3h Amplitude TP10 .6 volts. Amplitude TP11 16 volts.



Graph 2

3i Resistance RP12 Infinite ohms.

3j (1) Common Emitter Amplifier. (2) (b) Open R12

31 (1) decreased to 0, DC voltage (2) open, shorted

3n (1) cutoff (2) R12, R11 (3) increase, impaired (4) does, does
(5) increase, increases, infinity

If your response to ANY of the statements is wrong, or if ANY of your measurements are more than 10% different, go back and repeat that portion of the project. If necessary, review the referenced text material for clarification. Your instructor will assist if needed.

CONSULT YOUR INSTRUCTOR FOR THE PROGRESS CHECK.

YOU MAY STUDY ANOTHER RESOURCE OR TAKE THE MODULE SELF-CHECK.

ANSWERS TO MODULE SELF-CHECK.

1. cutoff, jump
2. 1/2, 5
3. 1, 2
4. d. value of R2, R3, and V_{CC}.
5. less, Q1 and R3, R2 and R3.
6. increase, increase, impaired

HAVE YOU ANSWERED ALL OF THE QUESTIONS CORRECTLY? IF NOT, REVIEW THE MATERIAL OR STUDY ANOTHER RESOURCE UNTIL YOU CAN ANSWER ALL QUESTIONS CORRECTLY. IF YOU HAVE, CONSULT YOUR INSTRUCTOR FOR FURTHER GUIDANCE.

342

PREPARE THE MAN

ATC PT 3AQR3X020-X
Prepared by Keesler TTC
KEP-PT-49

Technical Training

ELECTRONIC PRINCIPLES (MODULAR SELF-PACED)

MODULE 49

SOLID STATE TRAPEZOIDAL WAVEFORM GENERATOR

1 April 1975

AIR TRAINING COMMAND

7-10

Designed For ATC Course Use

ATC Keesler 6-1003

DO NOT USE ON THE JOB

343

DEPARTMENT OF THE AIR FORCE
Headquarters, Air Training Command
Randolph Air Force Base, Texas 78148

ATC PROGRAMMED TEXT KEP-PT-49
1 April 1975

This programmed text was prepared at Keesler Technical Training Center. It consists of one volume which analyzes the principles of the solid state trapezoidal waveform generator.

The program was designed for use in the basic airman electronic principles course 3AQR3X020-1. The material contained herein has been validated using airman students who met the course input criteria. Eighty percent of the students scored at least eighty percent on the master validation examination. The average student required 5 hours to complete the program.

PROGRAMMED TEXT

SOLID STATE TRAPEZOIDAL WAVEFORM GENERATORS

INSTRUCTIONS:

This text is made so that you will go through it step by step. Each frame, or step, will teach you a small bit of information. Answers for the questions for each frame are printed at the back of the text (in blocks).

Read the information and respond as you are directed. Turn to the back of the text and check your work. Do not proceed until you have responded correctly. If you need aid, see your instructor.

OBJECTIVES:

Solid State Trapezoidal Generators

a. Given the schematic diagram of a trapezoidal wave generator and a list of statements, select the statement that describes the effects on output linearity when time constants, applied voltage, and input gate duration are changed.

b. Given a trainer having a semiconductor trapezoidal wave generator circuit, multimeter, and oscilloscope, measure the output amplitude, rise time, and jump voltage within ± 10 percent accuracy.

c. Given a trainer with a malfunctioning trapezoidal wave generator circuit, a schematic diagram, multimeter, and oscilloscope, determine the faulty component two out of three times.

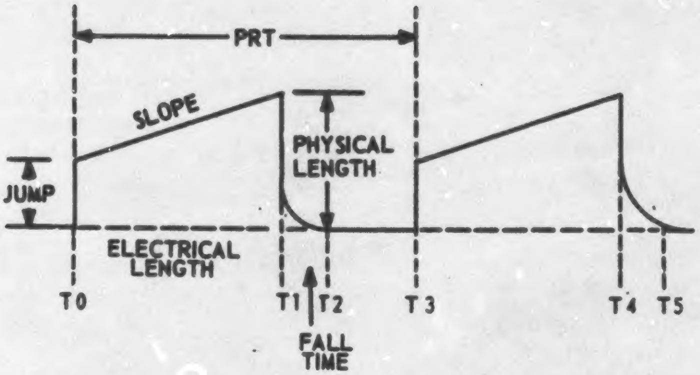
1. INTRODUCTION

Linearity, physical length, and electrical length in trapezoidal waveforms are changed by the same things as in the sawtooth generator we talked about in the last module. Linearity can be changed by two things: gate length, and the RC time constant. The simple proportion we used before can be used here. This is: $\text{Linearity} = \frac{RC}{\text{gate length}}$. You can see that linearity will increase if either R or C or both are increased. Also, linearity will decrease if either R or C, or both, are decreased. Linearity is inversely related to gate length, so if gate length is increased, linearity will decrease. The reverse is also true, that is, if gate length is decreased linearity will increase.

Physical length is also affected by changes in the RC time constant, gate length, or V_{CC}. If V_{CC} is increased, the capacitor will charge to a higher value but the percentage of charge will not change. This means that linearity can not change but physical length will increase. This is so because physical length is the voltage to which the capacitor charges. So remember, if V_{CC} increases, physical length increases.

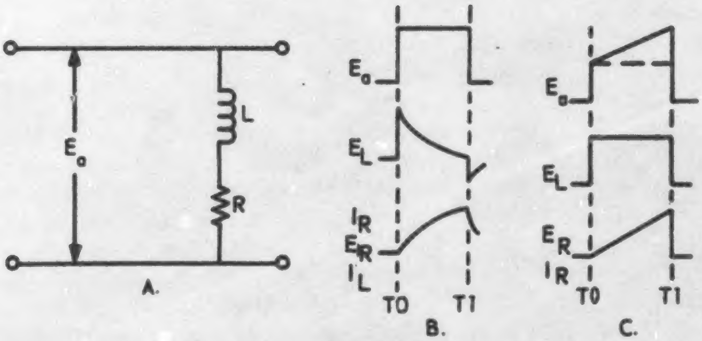
Electrical length is affected only by gate length. In fact, electrical length and gate length are always the same. This means that if gate length increases, electrical length increases.

Most oscilloscopes use electrostatic deflection. A sawtooth of voltage applied to the horizontal deflection plates will cause the electron beam to move. The beam will move horizontally. The CRTs in most TV and radar sets use an electromagnetic deflection system. Current flow in a coil around the neck of the CRT will cause the electron beam to move. A linear change of current will cause a linear movement of the beam. A sawtooth voltage wave applied to the deflection coils will not cause a linear change of current. A TRAPEZOIDAL voltage wave will cause a linear change of current in a deflection coil.


PRT
SLOPE
PHYSICAL LENGTH
JUMP
ELECTRICAL LENGTH
T0
T1
T2
T3
T4
T5
FALL TIME

REP4-2053

Figure 1


E_a
L
R
A.
E_a
E_L
I_R
E_R
I_L
T0
T1
B.
E_a
E_L
E_R
I_R
T0
T1
C.

REP4-1498

Figure 2

2. CHARACTERISTICS OF A TRAPEZOIDAL WAVE

Look at figure 1. It is a trapezoidal voltage waveform. It is the same as a sawtooth except for one thing; note the jump in voltage at time T0. This jump in voltage compensates for the DC resistance of the coil. The jump or step is followed by a linear rise of voltage to the peak. The time (measured in microseconds, milliseconds or seconds) from T0 to T1 is the electrical length. The fall time is the time for the voltage to drop from peak to zero (T1 to T2). The voltage amplitude at the peak point of the waveshape is referred to as the physical length. It is called the physical length because it is this amplitude which determines the physical movement of the electron beam on the CRT. The higher the amplitude, the greater the physical movement of the beam. The PRT is from T0 to T3 and the frequency of the wave is 1/PRT. The slope, as in a sawtooth wave, is part of the charge curve of a capacitor. The trapezoidal wave may be thought of as a sawtooth on top of a rectangular wave.

The jump voltage is required to overcome the internal resistance of a deflection coil. The coil resistance drops a voltage. The current through the resistance of the coil is proportional to the voltage drop across the resistance. A deflection coil and its resistance form a series RL circuit as shown in figure 2A. If you applied a square or rectangular wave of voltage across a coil with NO resistance the current rise would be linear.

However, all coils have resistance, and the result of applying a square wave to the coil in figure 2A is shown in figure 2B. At the first instant (T0), the coil acts as an open and drops all of the voltage. Current starts to flow and a voltage is developed across the resistance. As time passes, the voltage across the resistance increases and the voltage across the coil decreases. Note that E_R and E_L add up to E_a at all times. E_R, I_R, and I_L all follow the same curve, as shown in figure 2B. Notice the lack of linearity.

Figure 2C shows what happens when a trapezoidal voltage is applied to the coil. At T0 the jump voltage appears across the coil. E_R and I_R are zero at this point. Current now begins to flow and a voltage develops across R. As E_a increases, E_R and I_R increase AT THE SAME RATE. This keeps a constant voltage across the coil (E_L) and a linear rise of current takes place (I_R).

QUICK QUIZ 1:

1. Television and radar CRTs use an ________________ deflection system.

2. A sawtooth voltage applied to deflection coils will cause a linear increase of current. TRUE/FALSE.

3. A trapezoidal voltage waveform has the same characteristics as a sawtooth except for the __________ __________.

4. Current through a deflection coil is proportional to the voltage

   a. across the coil.

   b. across the coil resistance.

   c. applied across the coil and its resistance.

5. A trapezoidal voltage waveform applied to a deflection coil will cause a ________ ________________ increase of current.

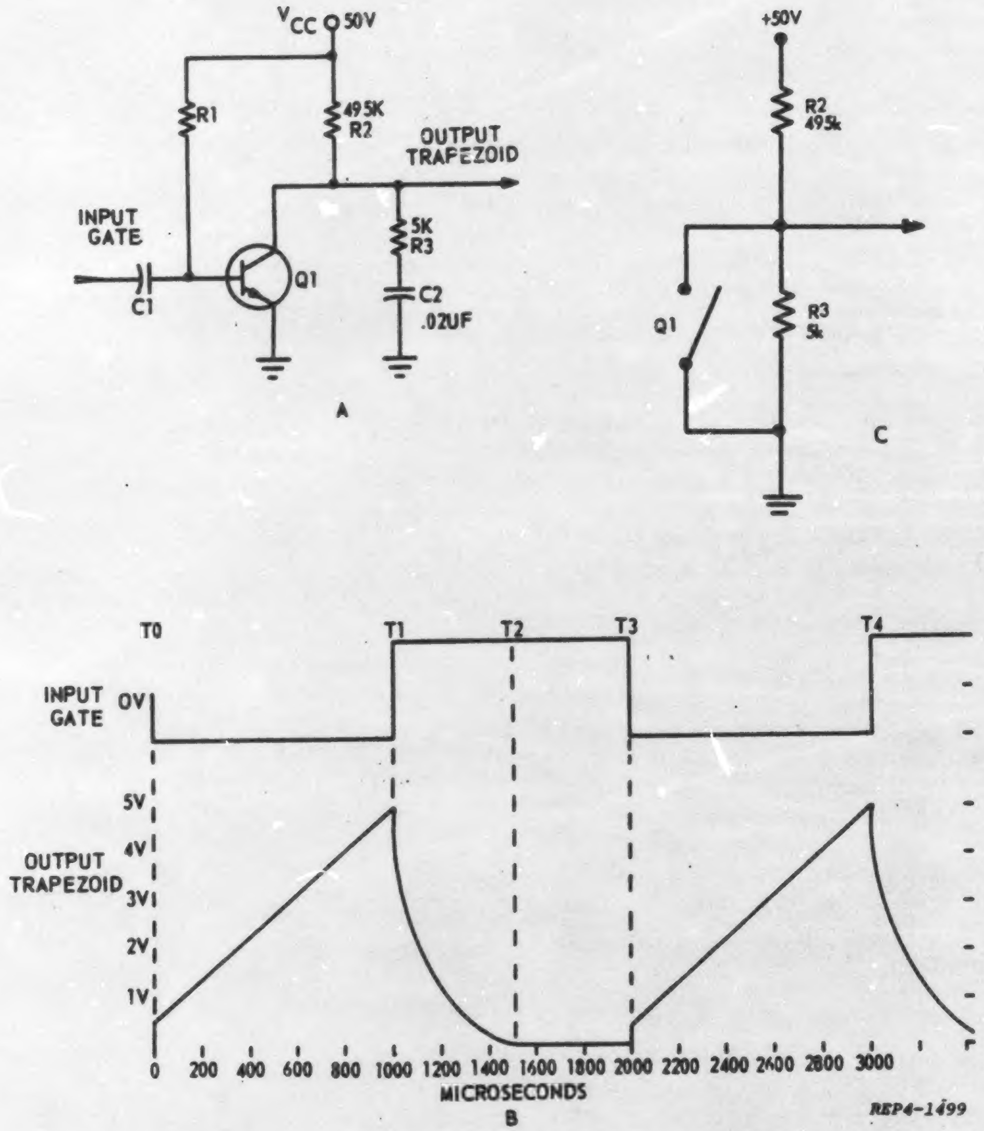

VCC 50V
R1
495K
R2
OUTPUT
TRAPEZOID
INPUT
GATE
C1
Q1
5K
R3
C2
.02UF
A
+50V
R2
495k
Q1
R3
5k
C
T0
T1
T2
T3
T4
INPUT
GATE
0V
5V
4V
OUTPUT
TRAPEZOID
3V
2V
1V
0
200
400
600
800
1000
1200
1400
1600
1800
2000
2200
2400
2600
2800
3000
MICROSECONDS
B
REP4-1499

Figure 3

3. TRANSISTOR TRAPEZOIDAL GENERATOR

A trapezoidal wave generator is shown in figure 3A. It is the same as a sawtooth generator except for R3, which is called a "jump" resistor. C1 couples the input gate to the base of Q1. R1 provides a forward bias path for Q1. R2 is the collector load resistor. R2, R3, and C2 form an RC network which determines the slope of the output. As in the sawtooth generator, Q1 acts as the switch. Figure 3B shows the input gate and the output trapezoid.

At time T0 (figure 3B) the negative gate is applied to the base of Q1 and cuts it off. Look at the output waveshape. The jump appears at this time. The reason for the jump is shown in figure 3C. This is the equivalent circuit at the time Q1 cuts off. C2 is not shown because the cutoff of Q1 is a very fast change and C2 acts as a short to the change. With C2 short, this leaves a simple series circuit made up of R2 and R3. The 50 volts applied divides across the two resistors in proportion to their size. R2 is 99 times as large as R3. This means that 99 percent of the voltage (49.5V) will be across R2 and 1 percent (.5V) across R3.

As the jump ends C2 starts to charge from ground through C2, R3 and R2, toward the applied 50V. C2 charges for the time the negative gate lasts, which is 1000 microseconds. The gate ends at time T1, and Q1 rapidly saturates. This causes C2 to discharge through Q1 and R3. As you can see from figure 3B, it takes about 500 microseconds for C2 to discharge and this is called the fall time. At T3 another negative gate is applied and the process is repeated.

The electrical length is the same length as the negative gate, or 1000 microseconds. The PRT is 2000 microseconds, and the frequency is 1/PRT. The time constant $R_2 + R_3$ and C2 is $500 \times 10^3 \times .02 \times 10^{-6}$ or 10,000 microseconds. To see if the slope is linear we can use the formula:

$$\#TC = \frac{TA}{RC} = \frac{1000 \times 10^{-6}}{500 \times 10^{3} \times .02 \times 10^{-6}}$$

$$= \frac{1000 \times 10^{-6}}{10{,}000 \times 10^{-6}} = .1$$

Since the capacitor only charges for .1 time constant (10%), the slope of the trapezoid is relatively linear. The physical length is also determined by the percentage of charge. The applied voltage is 50V and 10% of this is 5V. The physical length is therefore 5 volts.

QUICK QUIZ 2: Refer to figure 3:

1. The trapezoidal generator is the same as a sawtooth generator except for the ______ ______________ resistor.

2. The charge path for C2 is from ground thru C2, R3 and R2 to +50 volts. TRUE/FALSE.

3. The discharge path of C2 is from the negative side through Q1 and R3 to the positive side. TRUE/FALSE.

4. The input PRT is 2000 microseconds. The output frequency is therefore:

   a. 50 Hz

   b. 500 Hz

   c. 5000 Hz

   d. 50,000 Hz

5. At time T0 (figure 3B) C2 is short and the ______________ occurs.

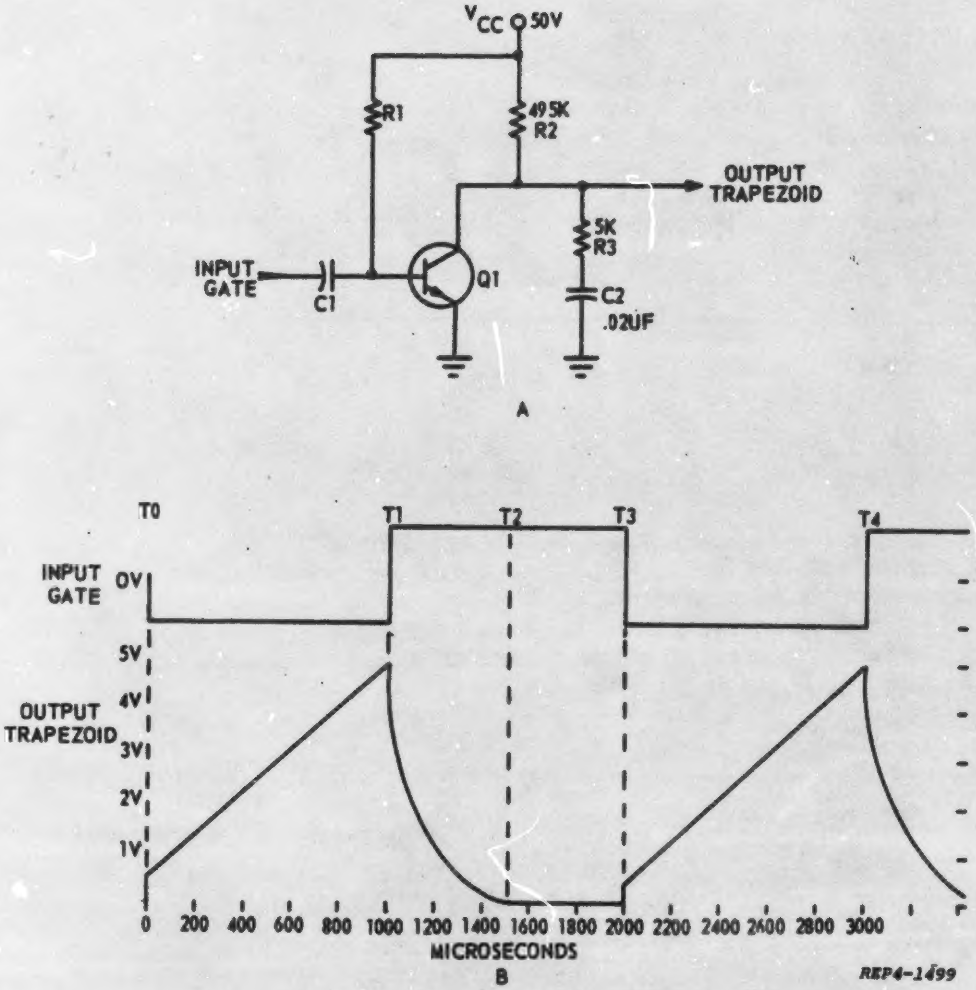
6. If R2 were 490 k ohms and R3 were 10 k ohms, the jump would be ____ V.

7. The fall time is the ____________ time of C2.

8. Considering Q1 as a switch, at time T0 the switch ______________ and at T1 it ______________.

9. C2 charges when Q1 is ON/OFF and discharges when Q1 is ON/OFF.

10. During the positive alternation of input, Q1 is __________.


VCC
50V
R1
495K
R2
OUTPUT
TRAPEZOID
5K
R3
INPUT
GATE
C1
Q1
C2
.02UF
T0
T1
T2
T3
T4
INPUT
GATE
0V
5V
4V
OUTPUT
TRAPEZOID
3V
2V
1V
0
200
400
600
800
1000
1200
1400
1600
1800
2000
2200
2400
2600
2800
3000
MICROSECONDS

A

B

REP4-1499

Figure 4

QUICK QUIZ 3: Refer to figure 4

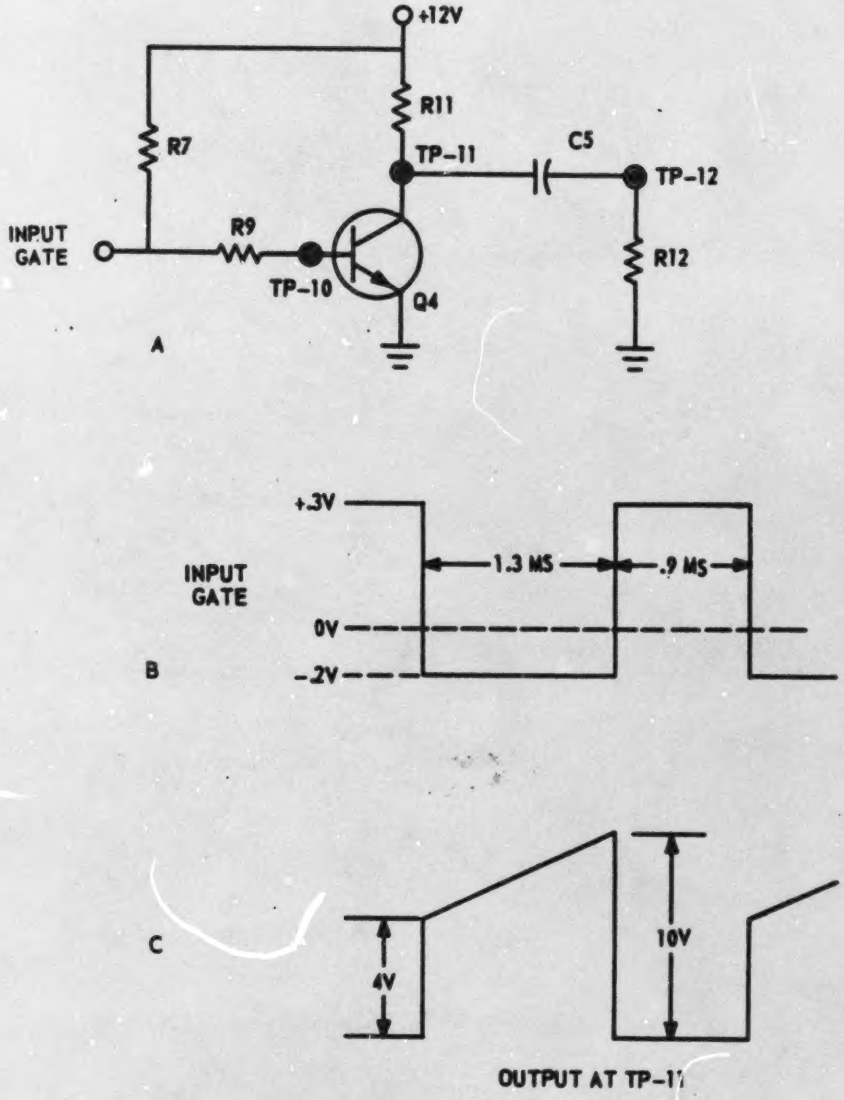
In the following questions determine whether linearity increases, decreases, or remains the same for the changes given.

1. R2 increases
2. R3 decreases
3. V_{CC} increases
4. C2 decreases
5. R2 + R3 increases
6. V_{CC} decreases
7. C2 increases
8. gate length increases
9. R2 decreases
10. R3 increases
11. R2 + R3 decreases
12. gate length decreases
13. R2, R3, C2 increases
14. R2, R3, C2 decreases

In the following questions, determine whether physical length increases, decreases, or remains the same for the changes given.

15. R2 increases
16. R3 decreases
17. V_{CC} increases
18. C2 decreases
19. R2 + R3 increases
20. V_{CC} decreases
21. C2 increases
22. gate length increases
23. R2 decreases
24. R3 increases
25. R2 + R3 decreases
26. gate length decreases
27. R2, R3, C2 increases
28. R2, R3, C2 decreases

351


+12V
R11
R7
TP-11
C5
TP-12
INPUT GATE
R9
TP-10
Q4
R12
A
+.3V
INPUT GATE
1.3 MS
.9 MS
0V
B
-.2V
C
4V
10V
OUTPUT AT TP-11

REP4-2054

Figure 5

4. TROUBLESHOOTING PROCEDURE

Troubleshooting the trapezoidal generator is the same as the sawtooth generator. The transistor is a common emitter amplifier. As before, when we speak of output, we mean an AC signal and not a straight line DC. As with the sawtooth generator, we will use the trainer circuit for troubleshooting. This circuit is shown in figure 5. It is, in fact, the sawtooth generator with jump resistor R12 added.

TROUBLE: No input gate.

SYMPTOMS: No output, no signal at the base of Q4.

ANALYSIS: With no gate being applied to Q4 there can be no output. There are several things which could prevent the signal from reaching the base of Q4. One of these is R9 open. If something happens in the preceding circuit, no signal can reach the base of Q4.

TROUBLE: Q4 open.

SYMPTOMS: No output, signal at the base of Q4 normal, V_C of Q4 = V_{CC}.

ANALYSIS: With Q4 open, no collector current can flow so there is no output and V_C of Q4 is at V_{CC}, however, the base signal should be normal.

TROUBLE: R11 open.

SYMPTOMS: No output, base signal normal, V_C of Q4 = 0.

ANALYSIS: There can be no collector current or voltage with R11 open so V_C of Q4 = 0. This trouble does not prevent the signal from being seen at the base of Q4.

TROUBLE: R12 open.

SYMPTOMS: Output is the input gate, inverted by 180° and amplified. Resistance reading from TP-12 to ground is infinite.

ANALYSIS: If R12 opens there is no charge path for C5. This makes Q4 a common emitter amplifier. The output is the input gate, inverted and amplified. The resistance reading from TP-12 to ground is infinite because you are reading across an open.

QUICK QUIZ 4: Refer to figure 5.

1. There is no output but the base signal is normal and V_C of Q4 equals zero volts. The trouble is

   a. Q4 open

   b. No input

   c. R11 open

   d. R9 open

2. The output is the input gate, amplified and inverted. The resistance from TP-12 to ground is infinite. The trouble could be

   a. Q3 short

   b. R12 open

   c. Q4 open

   d. R11 open

3. There is no output but the base signal is normal. V_C of Q4 = V_{CC}.

   a. no input

   b. R12 open

   c. R11 open

   d. Q4 open

4. There is no output and no signal at the base. The trouble could be

   a. Q3 short

   b. R11 open

   c. R12 open

   d. Q4 open

SUMMARY QUIZ:

1. Most television and radar CRTs use an electrostatic deflection system. TRUE/FALSE

2. A trapezoid voltage waveform has the same characteristics as a sawtooth except for the ________________

3. A trapezoid voltage applied to deflection coils will cause a linear rise of VOLTAGE/CURRENT.

4. Current through a deflection coil is proportional to the voltage

   a. across the coil

   b. across the coil resistance

   c. appled

5. The trapezoidal generator is the same as the sawtooth generator except for the COLLECTOR LOAD/JUMP resistor.

Refer to figure 3 or 4.

6. If R2 were 480 k ohms and R3 were 20 k ohms, the jump would be ________V.

7. During the negative alternation of the input, Q1 is ________________.

8. C2 charges when Q1 is OFF/ON.

9. The trapezoid is formed when C2 CHARGES/DISCHARGES and while Q1 is OFF/ON.

10. At time T0, C2 is a short and the ________ occurs.

11. The fall time is the charge time of C2. TRUE/FALSE.

In the following questions determine whether linearity increases, decreases, or remains the same for the changes given.

12. R2, R3, C2 increases

13. gate length decreases

14. R2, R3, C2 decreases

15. R2 + R3 decreases

16. R3 increases

17. R2 decreases

18. gate length increases

19. C2 increases

20. V_{CC} decreases

21. R2 + R3 increases

22. C2 decreases

23. V_{CC} increases

24. R3 decreases

25. R2 increases

Refer to figure 5 for questions 26 and 27.

26. There is no output and no signal at the base. The trouble may be

   a. Q4 open

   b. R1 open

   c. Q3 short

   d. R12 open

27. The output is the input gate, inverted and amplified. The resistance reading from TP-12 to ground is infinite. The trouble is

   a. R12 open

   b. Q4 open

   c. R11 open

   d. R9 open

ANSWERS TO QUICK QUIZ 1:

1. electromagnetic.
2. False
3. Jump voltage
4. b
5. linear

ANSWERS TO QUICK QUIZ 2:

1. jump
2. true
3. true
4. b
5. jump
6. 1 volt
7. discharge
8. opens, closes
9. off, on
10. saturated

ANSWERS TO QUICK QUIZ 3:

1. increases
2. decreases
3. remains the same
4. decreases
5. increases
6. remain the same
7. increases
8. decreases
9. decreases
10. increase
11. decrease
12. increase
13. increase
14. decrease
15. decrease
16. increase
17. increase
18. increase
19. decrease
20. decrease
21. decrease
22. increase
23. increase
24. decrease
25. increase
26. decrease
27. decrease
28. increase

ANSWERS TO QUICK QUIZ 4:

1. c
2. b
3. d
4. a

ANSWERS TO SUMMARY QUIZ:

1. False
2. jump
3. current
4. b
5. jump
6. 2
7. off
8. off
9. charges, off
10. jump
11. False
12. increases
13. increases
14. decreases
15. decreases
16. increases
17. decreases
18. decreases
19. increases
20. no change
21. increases
22. decreases
23. no change
24. decreases
25. increases
26. c
27. a

WHEN YOU HAVE COMPLETED THIS PROGRAMMED TEXT, AND CAN ANSWER ALL QUESTIONS CORRECTLY, PROCEED TO YOUR GUIDANCE PACKAGE, KEP-GP-49, PAGE 9, AND DO LABORATORY EXERCISE 49-1 ON SOLID STATE TRAPEZOIDAL GENERATORS.

356

PREPARE THE MAN

ATC GP 3AQR3X020-X
Prepared by Keesler TTC
KEP-GP-50

Technical Training

ELECTRONIC PRINCIPLES (MODULAR SELF-PACED)

MODULE 50

SOLID STATE LIMITERS AND CLAMPERS

1 September 1975

AIR TRAINING COMMAND

7-10

Designed For ATC Course Use

C Keesler 6-0300

DO NOT USE ON THE JOB

Radar Principles Branch
Keesler Air Force Base, Mississippi

ATC GP 3AQR3X020-X
KEP-GP-50
1 September 1975

ELECTRONIC PRINCIPLES (MODULAR SELF-PACED)

MODULE 50

SOLID STATE LIMITERS AND CLAMPERS

This Guidance Package is designed to guide you through this module of the Electronic Principles Course. This Guidance Package contains specific information, including references to other resources you may study, enabling you to satisfy the learning objectives.

CONTENTS

Title	Page
Overview	1
List of Resources	1
Adjunct Guide	1
Laboratory Exercise 50-1	9
Laboratory Exercise 50-2	13
Module Self-Check	17
Answers	19

OVERVIEW

1. SCOPE: Limiter circuits find their primary applications in waveshaping and protection. Clampers, on the other hand, are used primarily to change the reference point of either the upper or lower limits of the input signal. Numerous methods are used in reaching the desired result; how the result is reached is our goal during this module of training. You will also learn to identify output signals with a given input, and what effect changes in bias have on the output.

2. OBJECTIVES: Upon completion of this module you should be able to satisfy the following objectives:

a. Given the input waveform to the following solid state diode limiters and a group of output waveforms, select the waveform that would be present at the output of the named diode limiter.

(1) Series Positive
(2) Series Negative
(3) Shunt Negative with bias
(4) Shunt Positive with bias

b. Given schematic diagrams of biased diode shunt limiters and a list of statements, select the statement that describes the effect on limiting when bias is changed.

c. Given the input waveform to a zener diode limiter, a specified breakdown voltage, and a group of output waveforms, select the waveform that would be present at the output.

d. Given the schematic diagram of a transistor limiter and a list of statements, select the statement that describes the effect on limiting when bias is changed.

e. Given the input waveform to the following solid state diode clampers and a group of output waveforms, select the waveform that would be present at the output of the named diode clamper.

(1) Negative with bias
(2) Positive with bias

Supersedes KEP-GP-50, 1 February 1975.

f. Given a trainer having a limiter, schematic diagram, oscilloscope, and multimeter, determine the effect on limiting when bias is changed.

g. Given a trainer having a clamper, schematic diagram, oscilloscope, and multimeter, determine the effect on the voltage reference when the bias is changed.

LIST OF RESOURCES

To satisfy the objectives of this module, you may choose according to your training, experience, and preference, any or all of the following.

READING MATERIALS:

Digest

Adjunct Guide and Student Text VI

AUDIOVISUALS:

Television Lesson 30-504, Triode Limiters

Television Lesson 30-505, Duodiode Limiters (TSTR)

LABORATORY EXERCISES:

Laboratory Exercise 50-1, Solid State Limiters

Laboratory Exercise 50-2, Solid State Clampers

AT THIS POINT, IF YOU FEEL THAT THROUGH PREVIOUS EXPERIENCE OR TRAINING YOU ARE FAMILIAR WITH THIS SUBJECT, YOU MAY TAKE THE MODULE SELF-CHECK.

CONSULT YOUR INSTRUCTOR IF YOU NEED HELP.

ADJUNCT GUIDE

INSTRUCTIONS:

* Study the referenced materials as directed.

Return to this guide and answer the questions.

Check your answers against the answers at the back of this Guidance Package.

Contact your instructor if you experience any difficulty.

Begin the program.

A. Turn to Student Text, Volume VI, and study paragraphs 7-1 through 7-16. Return to this page and answer the following statements/questions.

1. The two primary purposes of limiter circuits are:

a. ______________________________

b. ______________________________

2. A negative limiter removes all or a portion of the (negative) (positive) half cycle of the input signal, and a positive limiter removes all or a portion of the (negative) (positive) half cycle.

3. The key for identification of a series limiter is the diode in (series) (parallel) with the output signal.

4. The diode of a series positive limiter will be (reverse) (forward) biased by the positive half of an input sine wave.

5. The diode of a series negative limiter will be (forward) (reverse) biased by the positive half of an input sine wave.

CONFIRM YOUR ANSWERS ON THE BACK PAGES.

B. Turn to Student Text, Volume VI, and study paragraphs 7-17 through 7-24. Return to this page and answer the following statements/questions.

1. The identification key for a shunt diode limiter is that the diode is in (series) (parallel) with the load.

2. The diode of a shunt positive limiter is (forward) (reverse) biased during the negative half of an input sine wave.

3. The diode of a shunt negative limiter is (forward) (reverse) biased during the negative half of an input sine wave.

CONFIRM YOUR ANSWERS ON THE BACK PAGES.

C. Turn to Student Text, Volume VI, and study paragraphs 7-25 through 7-39. Return to this page and answer the following statements/questions.

1. Refer to figure 50-1. Given circuit diagrams of solid state limiters with bias and input signals, match the waveforms in column B with the circuits in column A.

2. Study figure 50-1 and match the circuit diagrams in column A with the following list of limiter types.

a. Double diode limiter ______________

b. Negative limiter with positive bias ______________

c. Positive limiter with negative bias ______________

d. Positive limiter with positive bias ______________

e. Negative limiter with negative bias ______________

3. Refer to figure 50-1, schematic diagram c. Increasing the battery voltage of B2 to 8 volts would cause _______.

a. positive limiting to decrease.

b. positive limiting to increase.

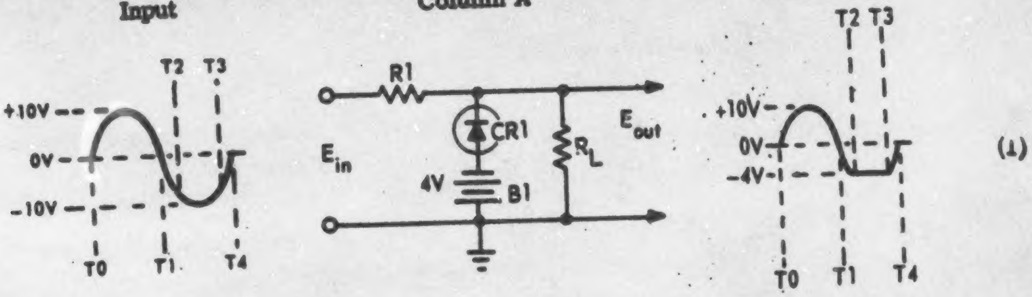
c. negative limiting to decrease.

d. negative limiting to increase.

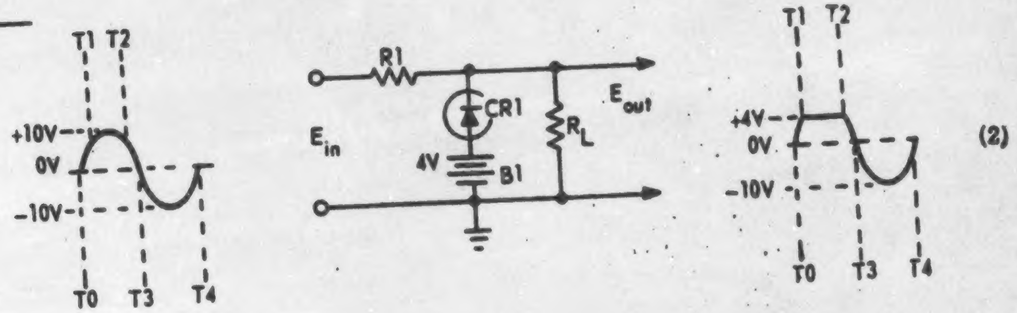
4. In reference to figure 50-1, circuit b, increasing the battery voltage to 6 volts would cause limiting to (increase) (decrease).

CONFIRM YOUR ANSWERS ON THE BACK PAGES.

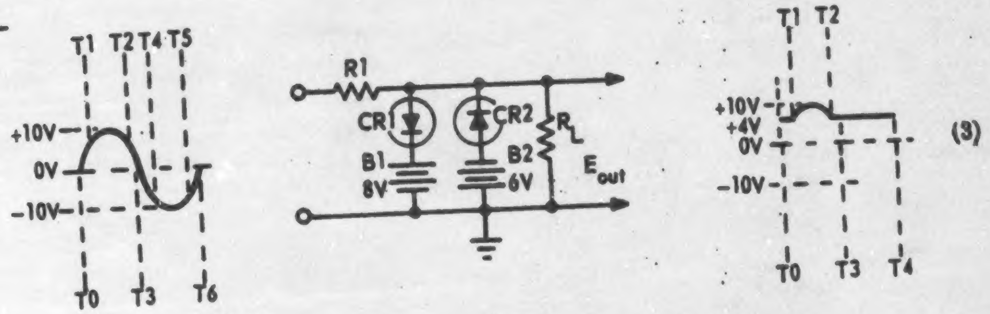
Input Column A Column B


T2
T3
+10V
0V
-10V
T0
T1
T4
R1
CR1
Ein
4V
B1
RL
Eout
T2 T3
+10V
0V
-4V
T0
T1
T4
(1)

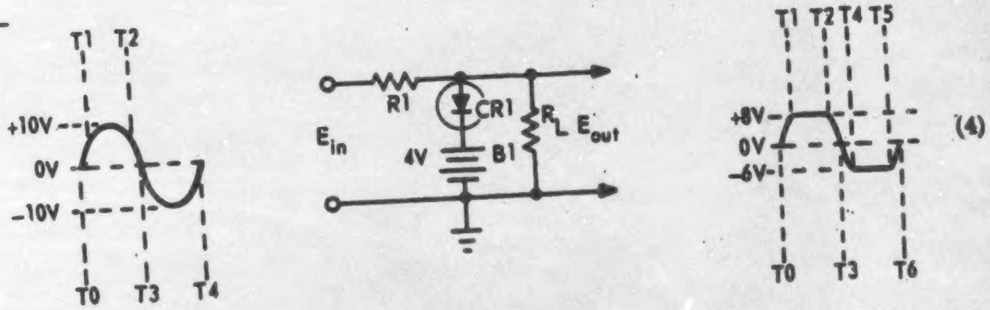
a. ____


T1 T2
+10V
0V
-10V
T0
T3
T4
R1
CR1
Ein
4V
B1
RL
Eout
T1 T2
+4V
0V
-10V
T0
T3
T4
(2)

b. ____


T1 T2 T4 T5
+10V
0V
-10V
T0
T3
T6
R1
CR1
B1
8V
CR2
B2
6V
RL
Eout
T1 T2
+10V
+4V
0V
-10V
T0
T3
T4
(3)

c. ____


T1 T2
+10V
0V
-10V
T0
T3
T4
R1
CR1
Ein
4V
B1
RL
Eout
T1 T2 T4 T5
+8V
0V
-6V
T0
T3
T6
(4)

d. ____

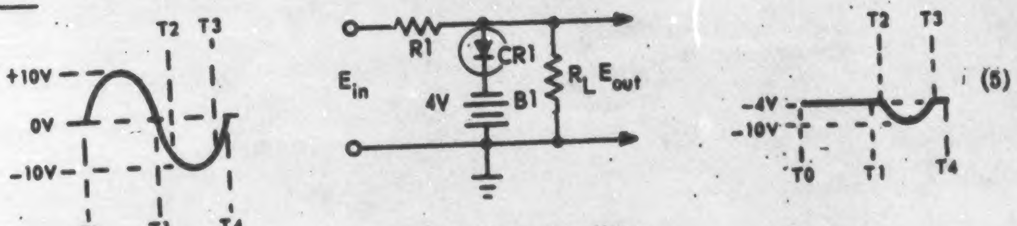

T2 T3
+10V
0V
-10V
T0
T1
T4
R1
CR1
Ein
4V
B1
RL
Eout
T2 T3
-4V
-10V
T0
T1
T4
(5)

Figure 50-1. Diode Limiters

e. ____

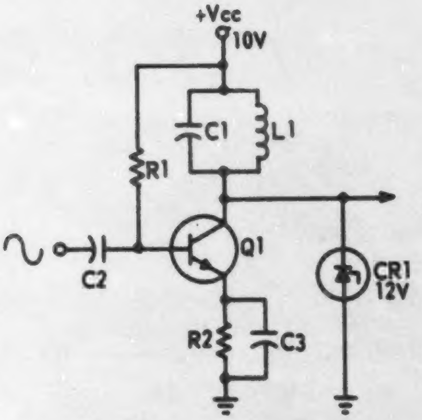

+Vcc
10V
C1
L1
R1
Q1
C2
CR1
12V
R2
C3

Figure 50-2. Transistor Limiter

D. Turn to Student Text, Volume VI, and study paragraphs 7-40 through 7-45. Return to this page and answer the following statements/questions.

1. Refer to figure 50-2. In this circuit, limiting of the output signal would occur if the collector voltage attempted to go above

_______ volts positive.

2. Which of the circuits shown in figure 50-3 would provide the output signal shown?

CONFIRM YOUR ANSWERS ON THE BACK PAGES.

E. Turn to Laboratory Exercise 50-1. You will perform various actions that will demonstrate how limiting is accomplished by various diode connections. You will also see how changes in bias will affect the degree of limiting.

Return and continue with this program when the Laboratory Exercise has been completed.

F. Turn to Student Text, Volume VI, and study paragraphs 7-46 through 7-76. Return to this page and answer the following statements/questions.

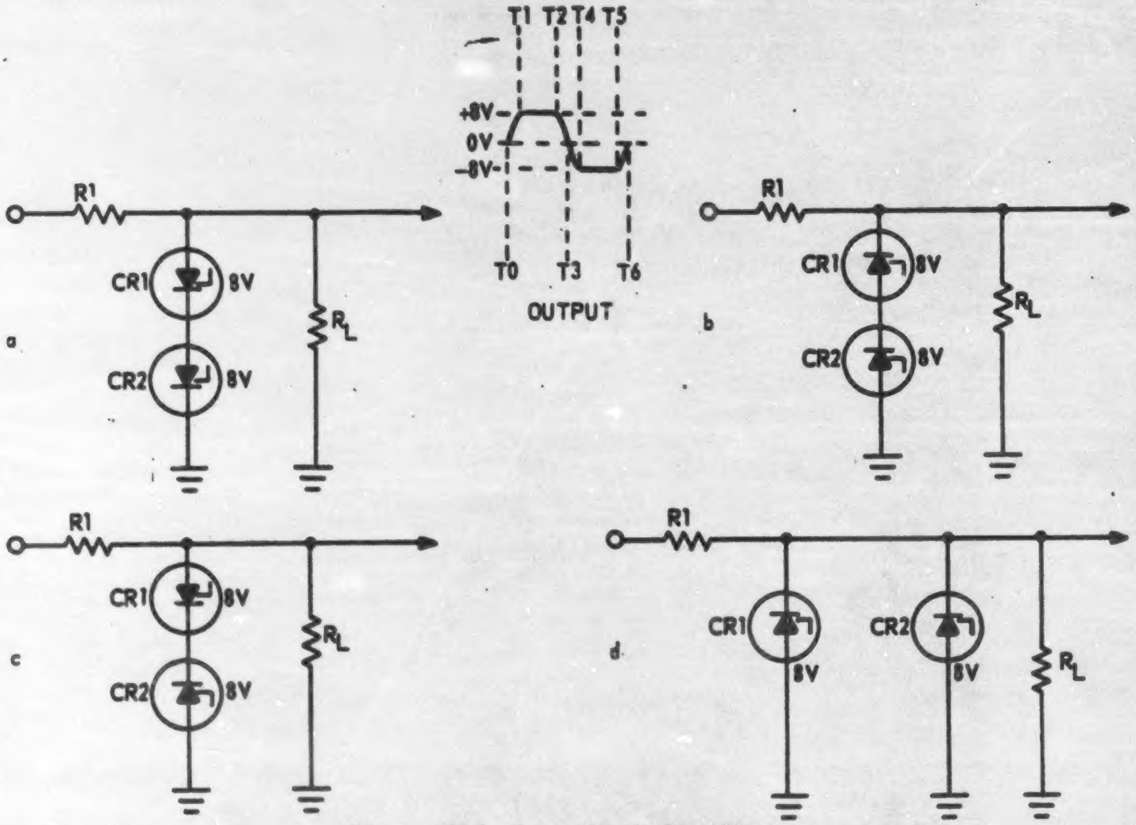

T1 T2 T4 T5
+8V
0V
-8V
T0 T3 T6
OUTPUT
a
R1
CR1 8V
CR2 8V
RL
b
R1
CR1 8V
CR2 8V
RL
c
R1
CR1 8V
CR2 8V
RL
d
R1
CR1 8V
CR2 8V
RL

Figure 50-3. Zener Diode Limiters

REP4-1500

1. Given a list of circuit names (a through f), select the correct name for each of the circuits illustrated in figure 50-4 (1 through 4). Enter your selection in the space to the left of each schematic.

- a. NPN saturation limiter
- b. NPN cutoff limiter
- c. NPN overdriven limiter
- d. PNP saturation limiter
- e. PNP cutoff limiter
- f. PNP overdriven limiter

(1) ____________

(2) ____________

(3) ____________

(4) ____________

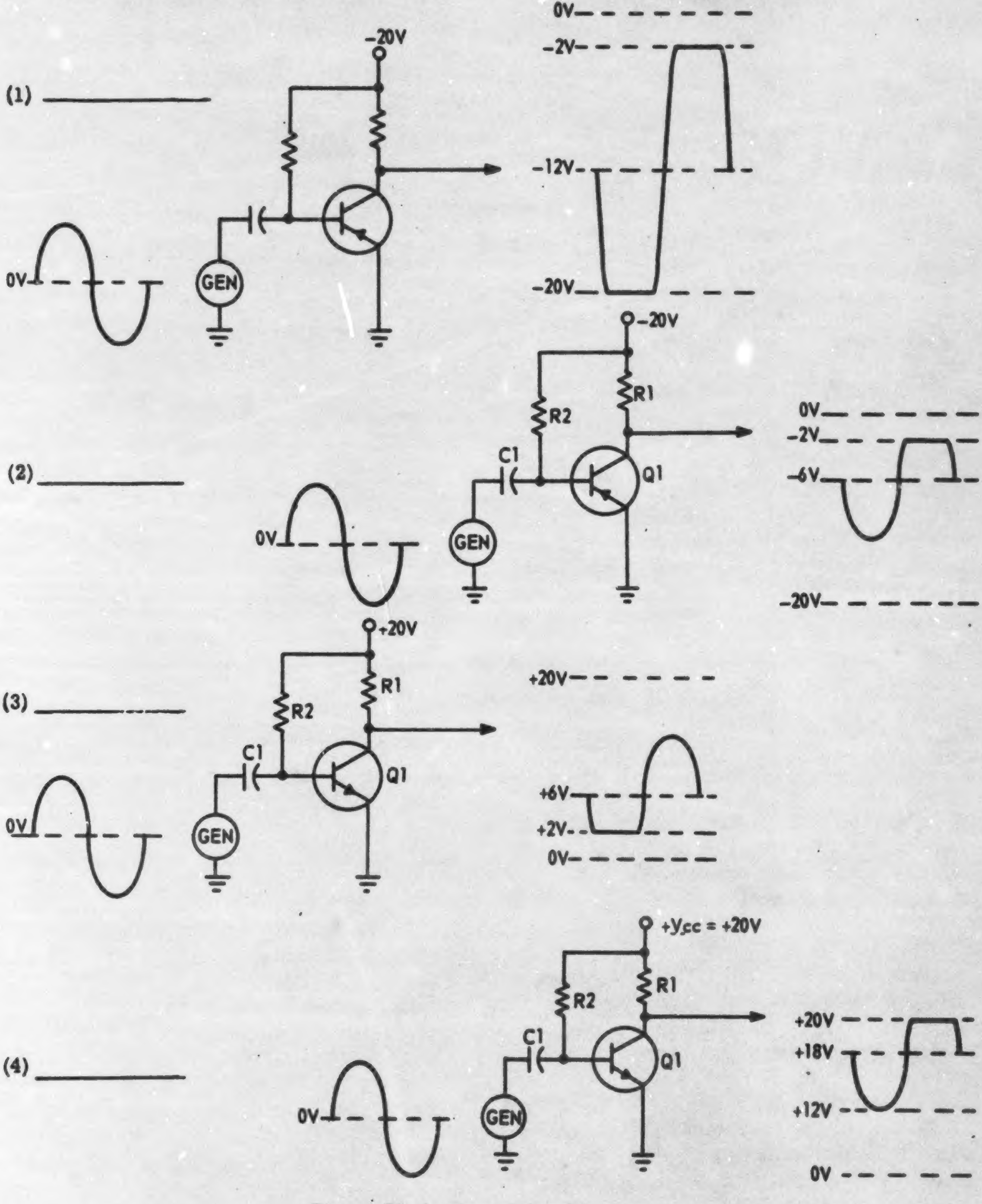

0V
-2V
-20V
-12V
0V
GEN
-20V
-20V
R1
R2
C1
Q1
0V
-2V
-6V
0V
GEN
-20V
+20V
R1
R2
C1
Q1
+20V
+6V
+2V
0V
0V
GEN
+Vcc = +20V
R1
R2
C1
Q1
+20V
+18V
+12V
0V
GEN
0V

Figure 50-4. Transistor Limiters

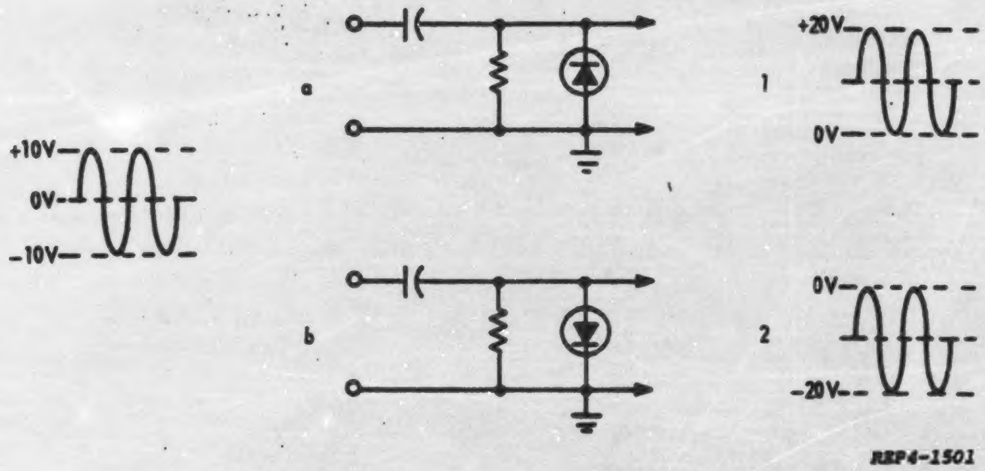


Figure 50-5. Diode Clampers

2. Refer to schematic diagram number (1) of figure 50-4. Increasing the forward bias of this circuit would (increase) (decrease) cutoff limiting and would (increase) (decrease) saturation limiting.

CONFIRM YOUR ANSWERS ON THE BACK PAGES.

G. Turn to Student Text, Volume VI, and study paragraphs 7-77 through 7-111. Return to this page and answer the following statements/questions.

1. A positive clamper without bias clamps the (lower) (upper) extremity of the output signal to 0 volts, and a negative clamper without bias clamps the (lower) (upper) extremity to 0 volts.

2. Match figure 50-5 schematic diagrams of positive and negative clampers having the same input signal with the output signals labeled 1 and 2.

a. ________________

b. ________________

3. Match figure 50-6 output waveshapes (1 and 2) to the appropriate clamper circuit.

a. __________________________

b. __________________________

CONFIRM YOUR ANSWERS ON THE BACK PAGES.

H. Turn to Student Text, Volume VI, and study paragraphs 7-112 through 7-132. Return to this page and answer the following statements/questions.

1. A positive clamper with positive bias clamps the (lower) (upper) extremity of the output wave to a (positive) (negative) potential.

2. A (positive) (negative) clamper with (positive) (negative) bias clamps the lower extremity of the output signal to a negative potential.

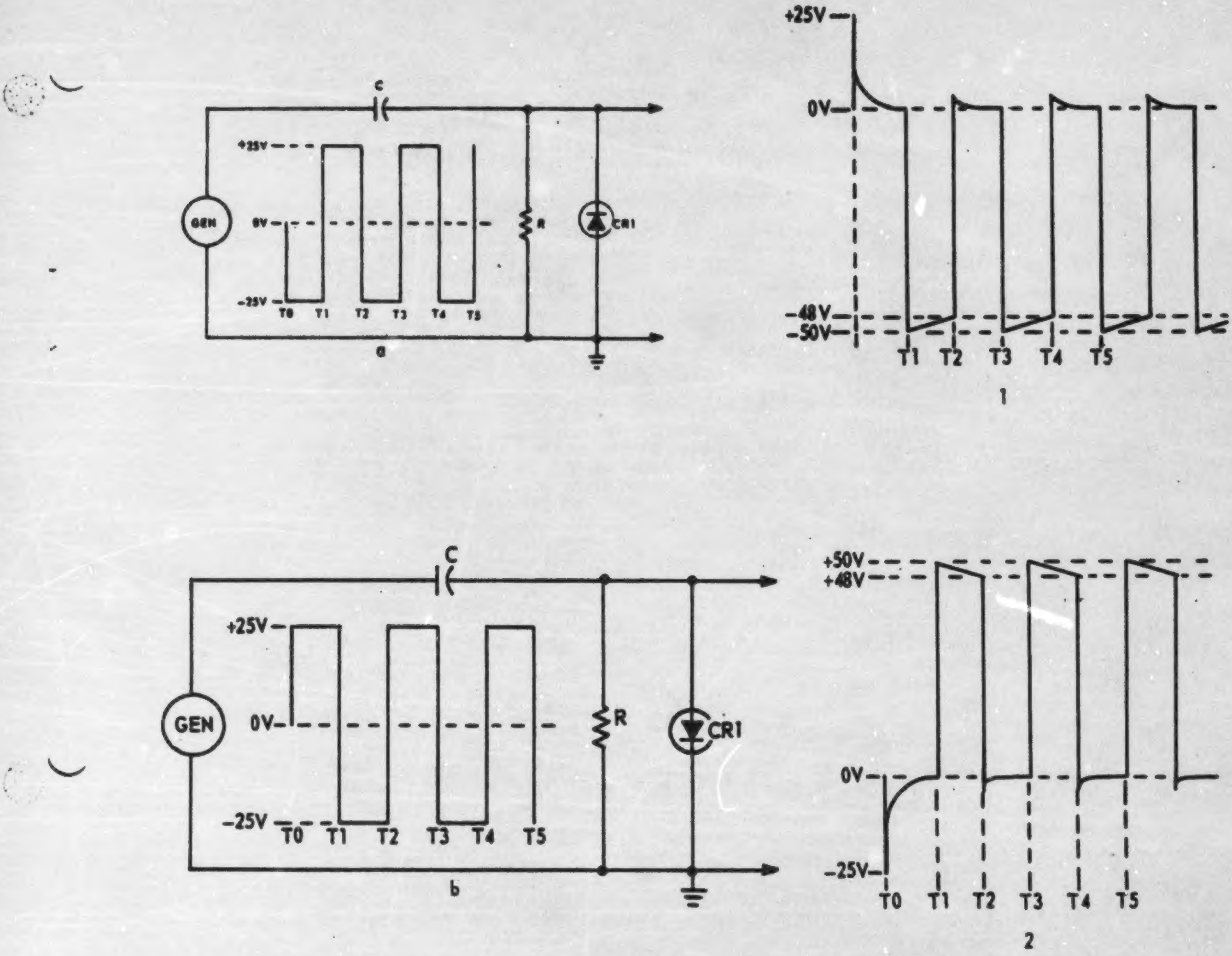

C
+25V
0V
-25V
GEN
T0
T1
T2
T3
T4
T5
R
CR1
a
+25V
0V
-48 V
-50V
T1
T2
T3
T4
T5
1
C
+25V
GEN
0V
-25V
T0
T1
T2
T3
T4
T5
R
CR1
b
+50V
+48V
0V
-25V
T0
T1
T2
T3
T4
T5
2

Figure 50-6. Diode Clampers

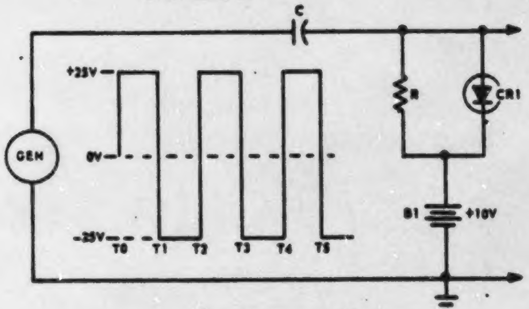
3. A negative clamper with negative bias clamps the (lower) (upper) extremity of the output signal to a (negative) (positive) potential.

4. A (positive) (negative) clamper with (positive) (negative) bias clamps the upper extremity of the output signal to a positive potential.

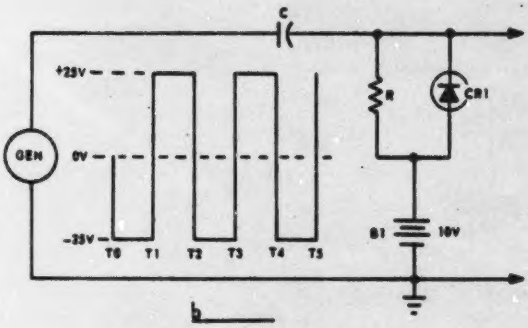
5. Match the circuit diagrams in column A with the signals they produce from column B of figure 50-7.

CONFIRM YOUR ANSWERS ON THE BACK PAGES.

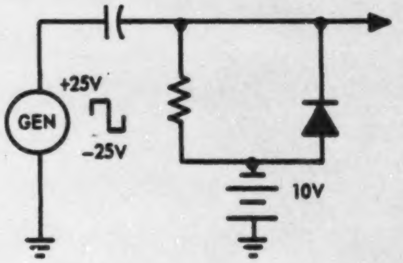
Column A


C
+25V
0V
-25V
T0
T1
T2
T3
T4
T5
GEN
R
CR1
B1
+10V

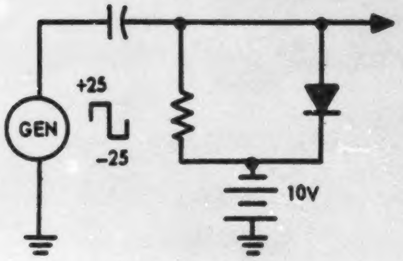
a ______


C
+25V
0V
-25V
T0
T1
T2
T3
T4
T5
GEN
R
CR1
B1
10V

b ______

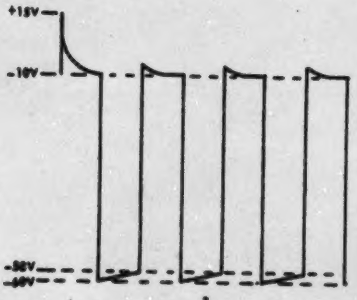

GEN
+25V
-25V
10V

c ______

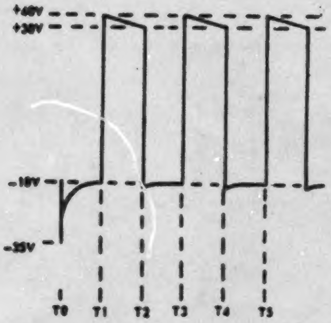

GEN
+25
-25
10V

d ______

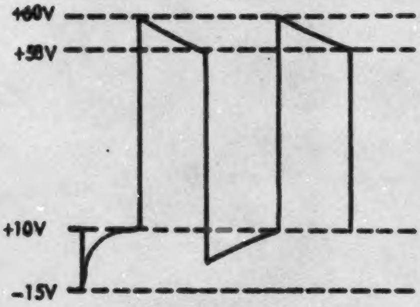
Column B



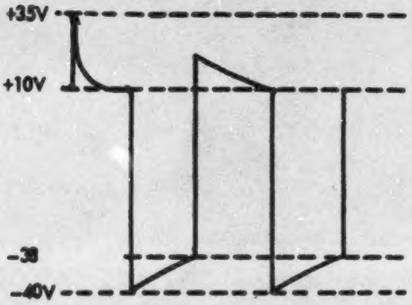
1



2



3



4

Figure 50-7. Biased Clampers

I. Turn to Laboratory Exercise 50-2. This project will allow you to prove the principles of biased and unbiased clampers which you have just learned.

YOU MAY STUDY ANOTHER RESOURCE OR TAKE THE MODULE SELF-CHECK.

LABORATORY EXERCISE 50-1

OBJECTIVE: Given a trainer having a limiter, schematic diagram, oscilloscope, and multimeter, determine the effect on limiting when bias is changed.

EQUIPMENT:

Limiters and Clampers Trainer (DD5925)

Oscilloscope

Multimeter

REFERENCE:

Student Text, Volume 6, paragraphs 7-1 through 7-39

CAUTION: OBSERVE BOTH PERSONNEL AND EQUIPMENT SAFETY AT ALL TIMES. REMOVE WATCHES AND RINGS.

PROCEDURES:

1. Trainer Analysis

Limiter circuits are widely used as signal shaping and protection circuits in all types of electronic applications. This trainer, by changing the various switches as directed, can be used as a simple, practical method of learning the operation of most types of diode limiters.

2. Equipment Preparation

a. Oscilloscope

Controls	Position
(1) Power	ON
(2) MODE	Alternate, or chopped
(3) POLARITY	Normal DC
(4) VOLTS/DIV (A & B)	2 volts (calibrated)
(5) TIME/DIV	5 millisecond (calibrated)
(6) TRIGGER SELECTOR	Auto, Line +
(7) HORIZONTAL POSITION	Normal Sweep
(8) FOCUS & INTENSITY	Clear Presentation
(9) POSITION	Adjust A sweep to first line from top of scope, and B channel to first line from bottom as zero references.

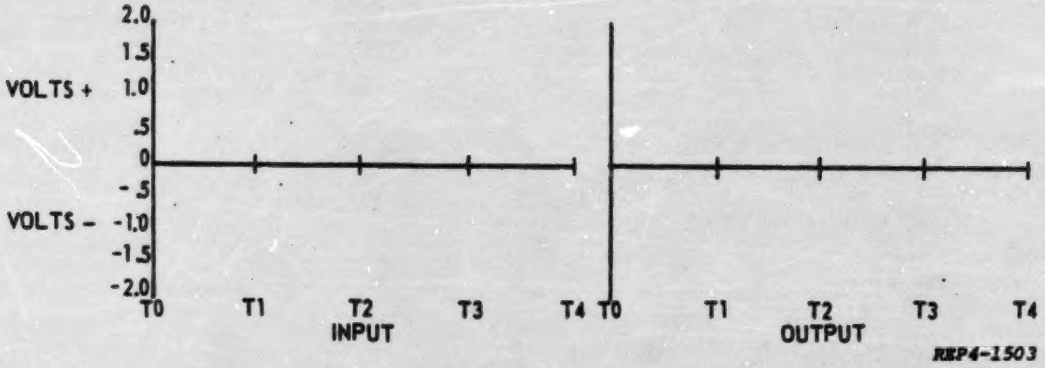
b. Trainer

Controls	Position
(1) S1	1
(2) S2	LO
(3) S3	3
(4) S4	4
(5) S5	1
(6) S6	1
(7) S7	1
(8) S8	2
(9) S9	+

c. Interconnections

(1) Ground trainer to oscilloscope.
(2) Connect A Channel probe to TP1.
(3) Connect B Channel probe to TP2.

d. Plug trainer into 110 volts AC.


2.0
1.5
VOLTS +
1.0
.5
0
-.5
VOLTS -
-1.0
-1.5
-2.0
T0
T1
T2
T3
T4
INPUT
T0
T1
T2
T3
T4
OUTPUT
REP4-1503

Graph 1-1

3. Activity

a. Adjust the vertical positioning controls so that the A Channel presentation is on the upper half of the oscilloscope face and the B Channel presentation is on the lower half.

b. Adjust the FOCUS and INTENSITY controls for a clear presentation on the oscilloscope.

c. Adjust R1 (amplitude control) on the trainer for a 4 volt peak to peak input signal (TP1, A Channel).

d. Measure the amplitude of the input and output signals and record your results.

Input __________ Pk-Pk

Output __________ Pk

e. Draw one cycle of the input and output signals on graph 1-1.

f. Underline the correct response to the following statements.

(1) The trainer is arranged as a (series) (shunt) (positive) (negative) limiter.

(2) The output signal is being developed across (CR2) (R3).

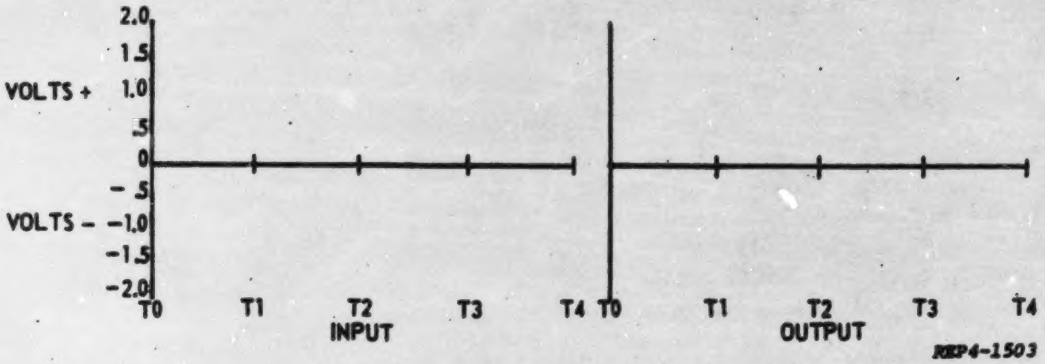
g. Change S3 to position 2.

h. Draw one cycle of the input and output signals on graph 1-2.

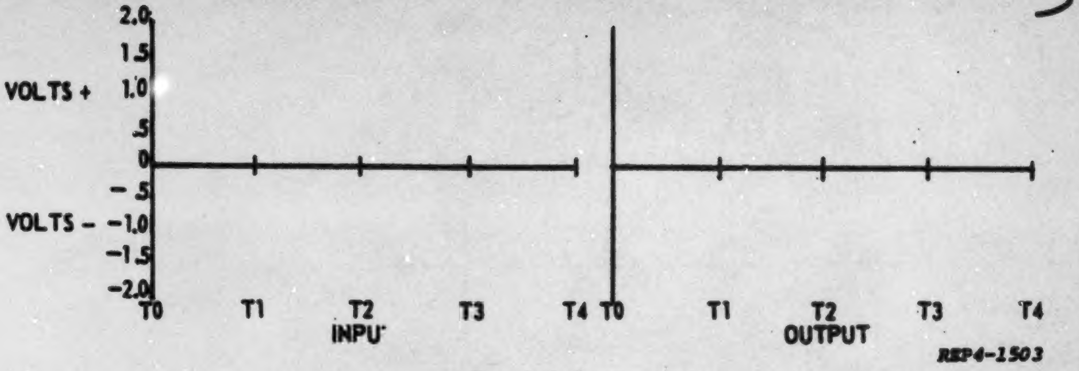
i. Underline the correct response to the following statements.

(1) The trainer has now been changed to a (series) (shunt) (positive) (negative) limiter.

(2) The output signal is being developed across (CR1) (R3).


2.0
1.5
VOLTS +
1.0
.5
0
-.5
VOLTS -
-1.0
-1.5
-2.0
T0
T1
T2
T3
T4
INPUT
T0
T1
T2
T3
T4
OUTPUT
REP4-1503

Graph 1-2



Graph 1-3

j. Change S3 to position 4 and S4 to position 2.

k. Draw one cycle of the input and output signals on graph 1-3.

l. Underline the correct response to the following statements.

(1) The trainer is now arranged as a (series) (shunt) (positive) (negative) limiter.

(2) (Positive) (Negative) (No) bias is being applied to the diode.

(3) The output signal is now being developed across (R2) (CR4) (R3).

m. Change S4 to position 3.

n. Draw one cycle of the input and output signals on graph 1-4.

o. Underline the correct response to the following statements.

(1) The trainer circuit has been changed to a (series) (shunt) (positive) (negative) limiter with (positive) (negative) (no) bias.

(2) The output signal is being developed across (R2) (CR3) (R3).

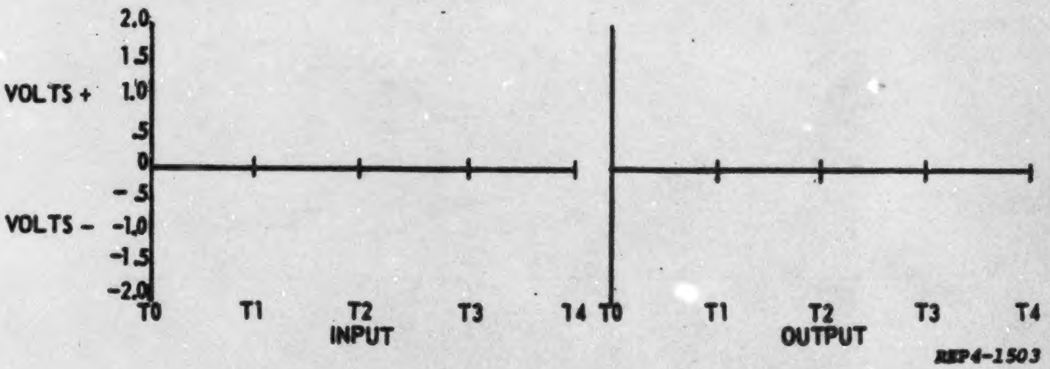
p. Change S5 to position 2.

q. Using the multimeter, measure the voltage at TP6 on the trainer and adjust R5 (bias control) for +1 volt DC (disconnect meter when finished).

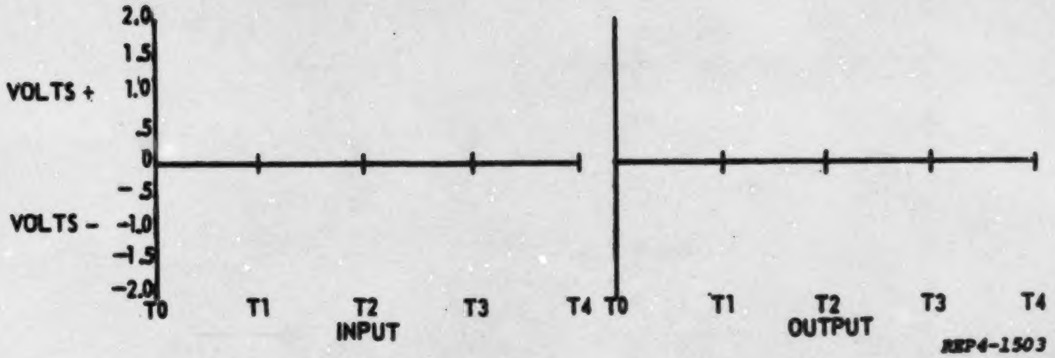
r. Using the oscilloscope, measure the input and output signal amplitude and record the results.

Input ____________________

Output ____________________



Graph 1-4



Graph 1-5

s. Draw one cycle of the input and output signals on graph 105.

t. Underline the correct response to the following statements.

(1) The trainer has been changed to a (series) (shunt) (positive) (negative) limiter with (positive) (negative) (no) bias.

(2) In this arrangement, the circuit is eliminating all of the (positive) (negative) input alternation and a portion of the (positive) (negative) alternation.

u. Change S9 to the - (negative) position.

v. Using the multimeter, measure the voltage at TP6 and adjust R5 (bias control) for -1 volt DC (disconnect meter when finished).

w. Draw one cycle of the input and output signals on graph 1-6.

x. Underline the correct response to the following statements.

(1) The trainer circuit is now arranged as a (series) (shunt) (positive) (negative) limiter with (positive) (negative) (no) bias.

(2) The degree of limiting is primarily determined by polarity and amount of bias connected to the diode. (True) (False)

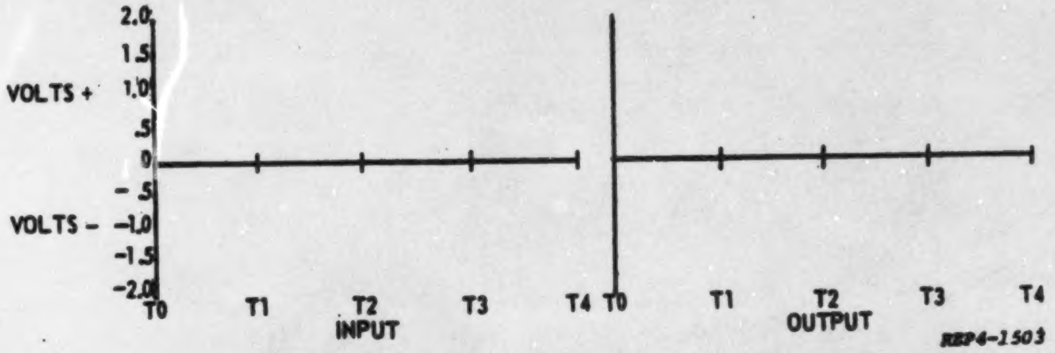
y. While observing the output signal on the oscilloscope, slowly vary the bias by turning R5 CW and CCW. Change S4 to position 2, S9 to + (positive), and repeat the bias variation.

z. Make a statement regarding your observations during step y.

____

____

CONFIRM YOUR RESPONSES ON THE BACK PAGES.



Graph 1-6

RETURN TO THE RESOURCE FROM WHICH YOU CAME AND CONTINUE WITH THAT PROGRAM.

LABORATORY EXERCISE 50-2

OBJECTIVE: Given a trainer having a clamper, schematic diagram, oscilloscope, and multimeter, determine the effect on the voltage reference when the bias is changed.

EQUIPMENT:

Limiters and Clampers Trainer (DD6925)

Oscilloscope

Multimeter

REFERENCE:

Student Text, Volume 6, paragraphs 7-77 through 7-131

PROCEDURES:

1. Trainer Analysis

By changing switch settings as directed, this trainer provides a simple, practical method for you to use in learning the operational theory of unbiased and biased clampers.

2. Equipment Preparation

a. Oscilloscope

Controls	Position
(1) Power	ON
(2) MODE	Alternate
(3) POLARITY	Normal, DC
(4) VOLTS/DIV	2, calibrated (change as required)
(5) TIME/DIV	1 millisecond, calibrated
(6) TRIGGER SELECTOR	Auto, Int, +

b.

Trainer	Position
(1) S1	2
(2) S2	LO
(3) S3	5
(4) S4	1
(5) S5	1
(6) S6	4
(7) S7	2
(8) S8	2
(9) S9	- bias (left)

c. Plug the trainer into 110 volts AC.

3. Activity

NOTE: For this project, the oscilloscope is used for measuring DC voltages. Therefore, it is recommended that you review Lab Project 20-3, Module 20, before continuing.

a. Establish 0 volts DC reference for A Channel on first line from the top of scope. Establish 0 volts DC reference for B Channel on second line from bottom of scope.

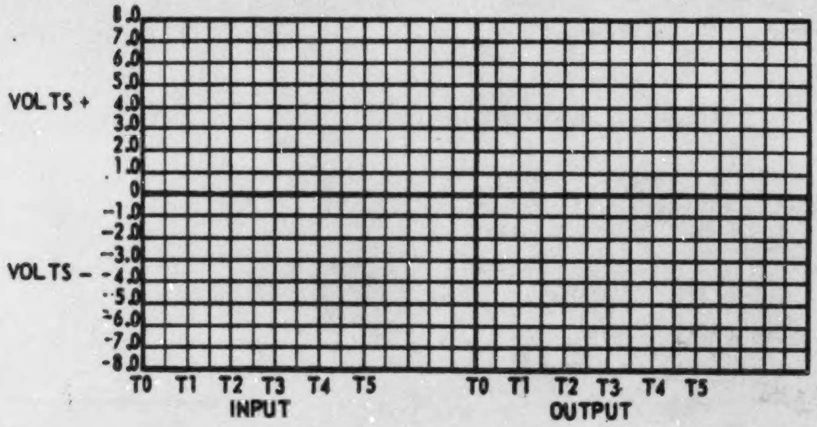
b. Connect A Channel probe to TP1, B Channel probe to TP3, and ground the oscilloscope to trainer at TP7.

c. Adjust input signal amplitude for 4 volts peak to peak.

d. Measure and record input and output signal amplitudes.

Input ________ Pk-Pk

Output ________ Pk



Graph 2-1

e. Draw two cycles of the input and output signals on graph 2-1.

f. Underline the correct response to the following statements.

(1) The trainer is arranged as a (positive) (negative) clamper with (positive) (negative) (no) bias.

(2) On the positive alternation of the input signal C3 (charged) (discharged) through (R4) (CR6).

(3) On the negative alternation of the input signal, C3

(a) completely discharged through CR6.

(b) completely discharged through R4.

(c) discharged slightly through R4.

g. While observing the input and output signals, vary the amplitude of the input signal up and down, and underline the correct response to the following statements.

(1) Both the negative and positive peaks of the input signal decreased toward zero as the amplitude was decreased. (True) (False)

(2) The most positive point of the output signal is (0) (+2) (+4) volts.

(3) As the input signal amplitude was decreased, the output positive peak remained at (0) (+2) (+4) volts and the negative peak (remained stationary) (decreased toward zero).

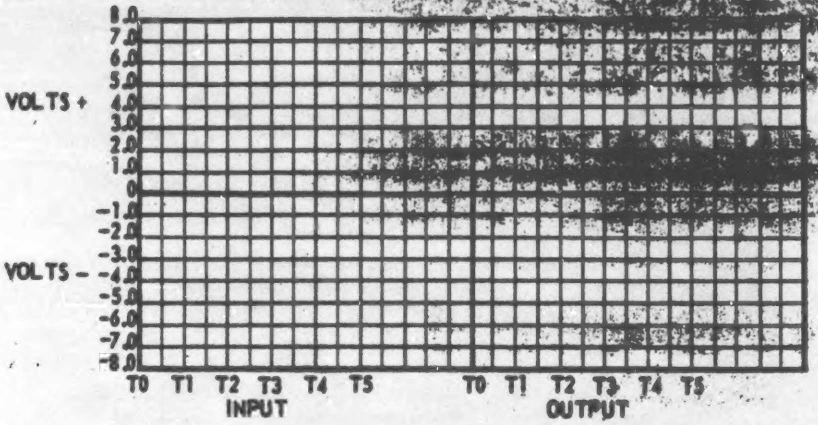
h. Readjust the input signal amplitude to 4 volts peak to peak and change S6 to position 2. Observe the output signal and underline the correct response to the following statements.

(1) The output signal (is) (is not) now distorted.

(2) The change in the output signal is caused by a/an (increase) (decrease) in circuit capacitance, causing a (faster) (slower) discharge through (R4) (CR6).

i. Change S6 to position 4 and S7 to position 3. Reestablish 0 reference for B Channel on bottom line of oscilloscope face.

j. While observing the output signal, vary the input signal amplitude up and down. Reset the input amplitude to 4 volts peak to peak, and draw two cycles of the output signal on graph 2-2.



Graph 2-2

k. Underline the correct response to the following statements.

(1) The circuit is now arranged as a (positive) (negative) clamper with (positive) (negative) (no) bias.

(2) The signal is now clamped from (-4) (0) (+4) volts in a (positive) (negative) direction.

l. Change S8 to position 1. Use the voltmeter to adjust the voltage at TP6 to -2 volts. Reestablish 0 volt reference for B Channel on first line from bottom of oscilloscope face.

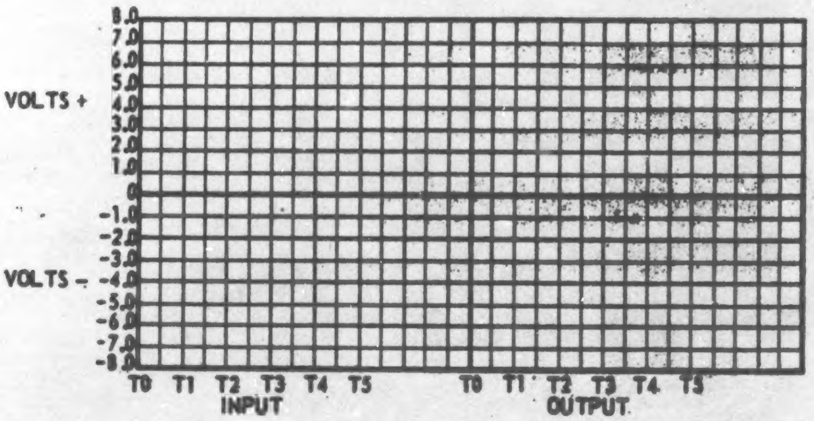
m. While observing the output signal, vary the input signal amplitude up and down. Reset the input amplitude to 4 volts peak to peak and draw two cycles of the input and output signals on graph 2-3.

n. Underline the correct response to the following statements.

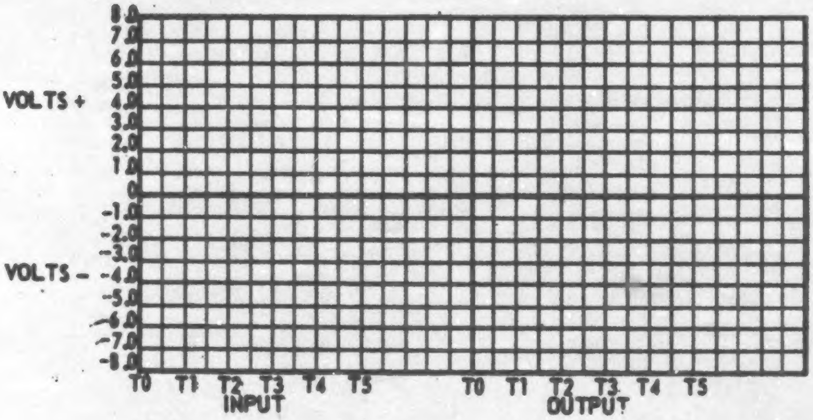
(1) The trainer is now arranged as a (positive) (negative) clamper with (positive) (negative) (no) bias.

(2) The (lower) (upper) extremity of the output signal is now clamped at (-2) (0) (+2) volts.

o. Change S9 to + (positive) and use the multimeter to adjust the voltage at TP6 to +2 volts. Reestablish 0 reference for B Channel on the bottom line of the oscilloscope face.



Graph 2-3



Graph 2-4

p. While observing the output signal, vary the input signal amplitude up and down. Reset the input amplitude to 4 volts peak to peak and draw two cycles of the input and output signals on graph 2-4.

q. Underline the correct response to the statements below.

(1) The trainer is now arranged as a (positive) (negative) clamper with (positive) (negative) (no) bias.

(2) The (upper) (lower) extremity of the output signal is clamped at (-2) (0) (+2) volts.

r. Summary

(1) A positive clamper always clamps the lower extremity of the output signal to a positive voltage. (True) (False)

(2) A negative clamper clamps the upper extremity of the output signal to a level determined by the bias applied to the diode. (True) (False)

(3) In a clamper circuit, using a capacitor that is too small will cause the output signal to be distorted. (True) (False)

(4) Both the upper and lower extremities of the input to a clamper will vary as the input amplitude is varied; however, only the lower OR upper extremity of the output will change. (True) (False)

CONFIRM YOUR ANSWERS ON THE BACK PAGES.

CONSULT YOUR INSTRUCTOR FOR PROGRESS CHECK.

YOU MAY STUDY ANOTHER RESOURCE OR TAKE THE MODULE SELF-CHECK.

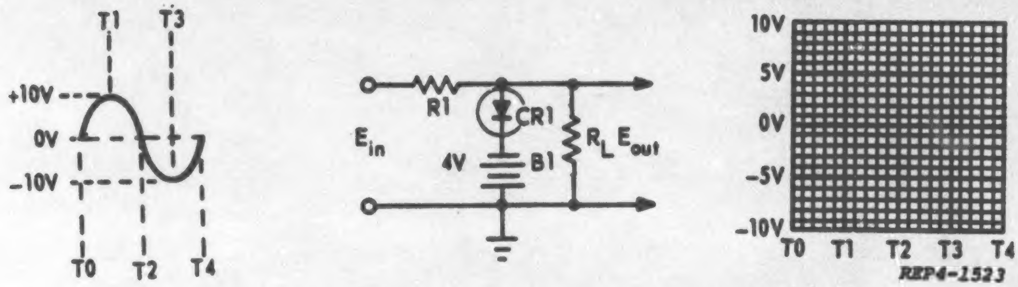

T1
T3
+10V
0V
-10V
T0
T2
T4
R1
CR1
E in
4V
B1
R L
E out
10V
5V
0V
-5V
-10V
T0
T1
T2
T3
T4
REP4-1523

Figure 50-8

MODULE SELF-CHECK

1. A series (negative) (positive) diode limiter will have (one) (two) positive pulse(s) across the output load for each cycle of input signal.

2. The diode of a shunt positive limiter is connected in (series) (parallel) with the load. During the period that a voltage is developed across the load, the diode is acting as (an open) (a closed) switch.

3. A series diode limiter will have an output developed when the input signal (forward) (reverse) biases the diode, and a shunt limiter will have an output developed when the input signal (forward) (reverse) biases the diode.

4. Given the circuit diagram and input signal shown in figure 50-8, draw the output signal on the graph.

5. The schematic diagram in figure 50-9 is correctly identified as a (positive) (negative) limiter with (positive) (negative) bias.

6. The circuit in figure 50-9 is correctly

identified as a ____________ ______________

________________ ________________.

7. Draw the output signal on the graph of figure 50-9 for the input shown.

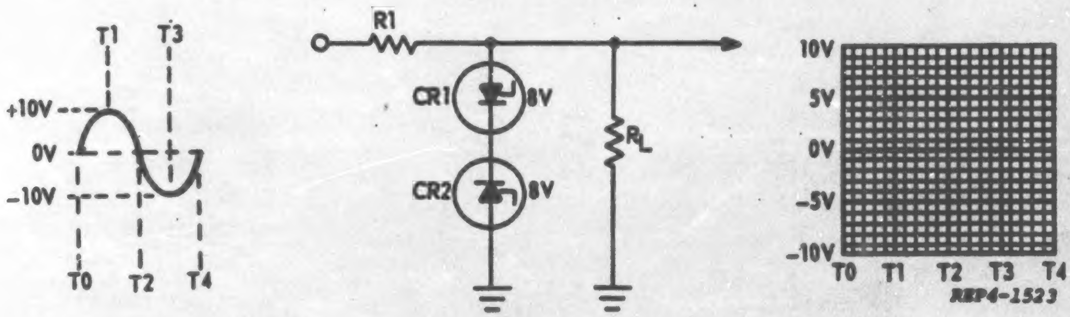

R1
T1
T3
+10V
0V
-10V
T0
T2
T4
CR1
8V
CR2
8V
R L
10V
5V
0V
-5V
-10V
T0
T1
T2
T3
T4
REP4-1523

Figure 50-9

375

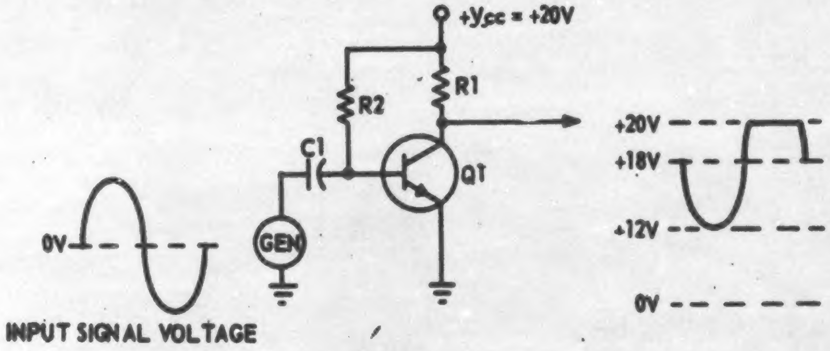

+Vcc = +20V
R1
R2
C1
Q1
GEN
0V
INPUT SIGNAL VOLTAGE
+20V
+18V
+12V
0V

Figure 50-10

8. Considering the input and output signals of the circuit in figure 50-10, the circuit would be correctly identified as a (NPN) (PNP) (cutoff) (saturation) limiter.

9. Increasing the forward bias in figure 50-10 would cause limiting to (increase) (decrease).

10. When the input signal to a transistor amplifier is of such an amplitude that the transistor is alternately driven to cutoff and saturation, the circuit becomes a/an

______________ limiter.

11. Basically, the purpose of a clamper circuit is to

a. double the input signal voltage.

b. double the input signal frequency.

c. fix the upper or lower signal extremity at a specified level.

d. change the waveshape of the input signal.

12. A positive clamper without bias will clamp the (upper) (lower) extremity of the output signal to (zero volts) (a positive value) (a negative value).

13. The circuit in figure 50-11 is correctly identified as a (negative) (positive) clamper with (negative) (positive) bias.

14. With the square wave input shown in figure 50-11, draw the circuit output signal on the graph provided.

CONFIRM YOUR ANSWERS ON THE BACK PAGES.

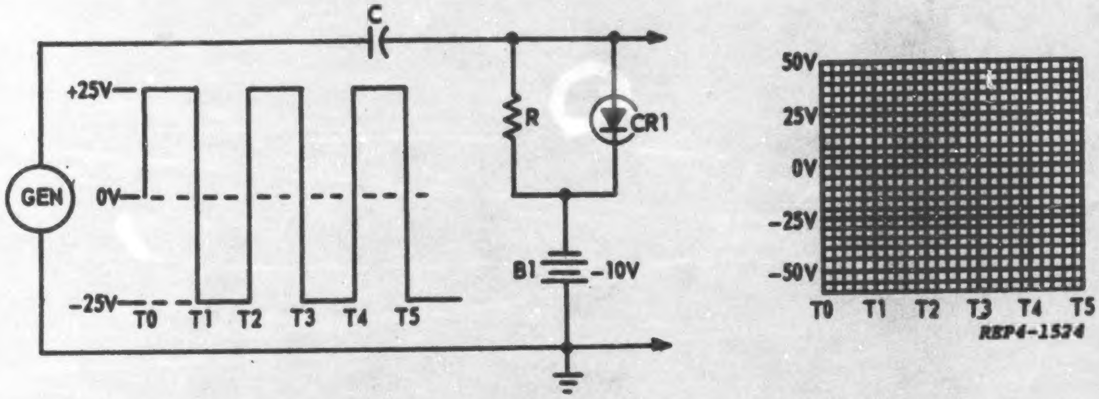

C
+25V
0V
-25V
T0
T1
T2
T3
T4
T5
GEN
R
CR1
B1
-10V
50V
25V
0V
-25V
-50V
T0
T1
T2
T3
T4
T5
REP4-1524

Figure 50-11

ANSWERS TO A:

1. a. waveshaping
   b. protection
2. negative, positive
3. series
4. reverse
5. forward

If you missed ANY questions, review the material before you continue.

ANSWERS TO B:

1. parallel
2. reverse
3. forward

If you missed ANY questions, review the material before you continue.

ANSWERS TO C:

1. a. (1)
   b. (3)
   c. (4)
   d. (2)
   e. (5)
2. a. c
   b. b
   c. e
   d. d
   e. a
3. c
4. increase

If you missed ANY questions, review the material before you continue.

ANSWERS TO D:

1. 12 volts
2. c

If you missed ANY questions, review the material before you continue.

ANSWERS TO F:

1. (1) f
   (2) d
   (3) a
   (4) b
2. decrease, increase

If you missed ANY questions, review the material before you continue.

ANSWERS TO G:

1. lower, upper
2. a. (1)
   b. (2)
3. a. (2)
   b. (1)

If you missed ANY questivns, review the material before you continue.

ANSWERS TO H:

1. lower, positive
2. positive, negative
3. upper, negative
4. negative, positive
5. a. (4)
   b. (3)
   c. (2)
   d. (1)

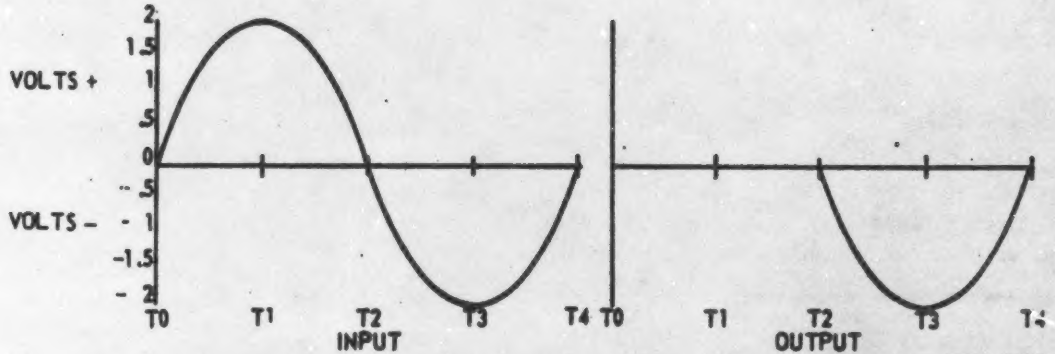
If you missed ANY questions, review the material before you continue.

ANSWERS TO LAB EXERCISE 50-1:

3. d. Input 4 volts peak to peak

Output 2 volts peak

e.



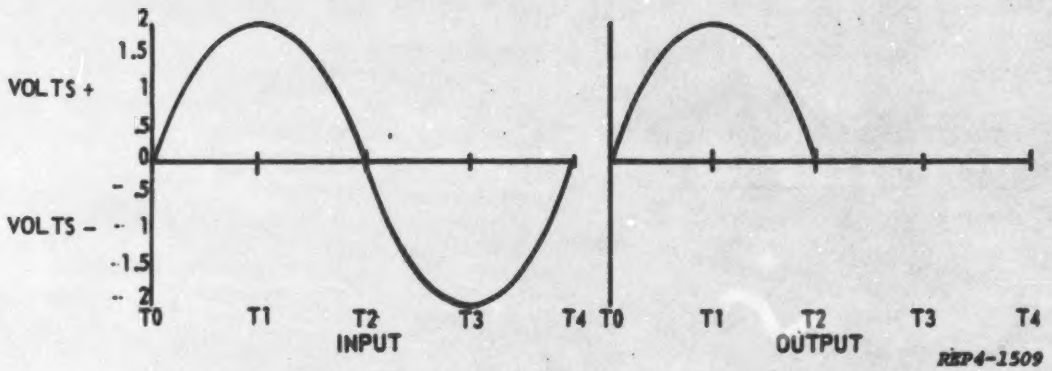
REP4-1508

Graph 1-1

f. (1) series, positive

(2) R3

h.



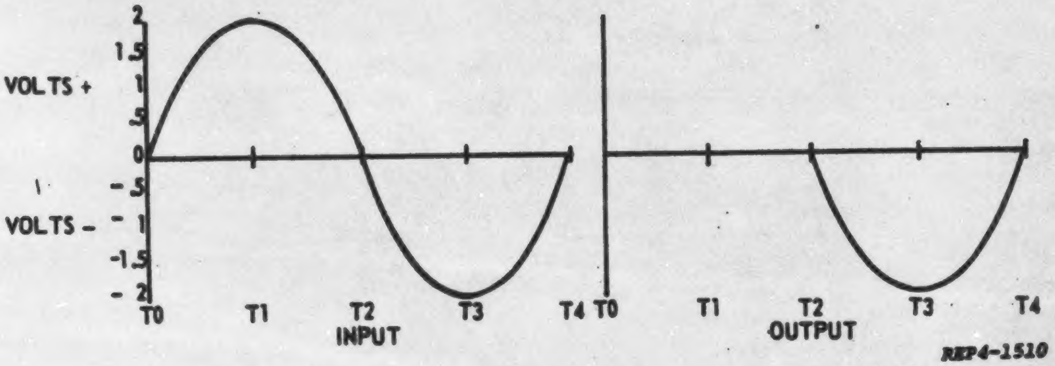
REP4-1509

Graph 1-2

i. (1) series, negative

(2) R3

k.



REP4-1510

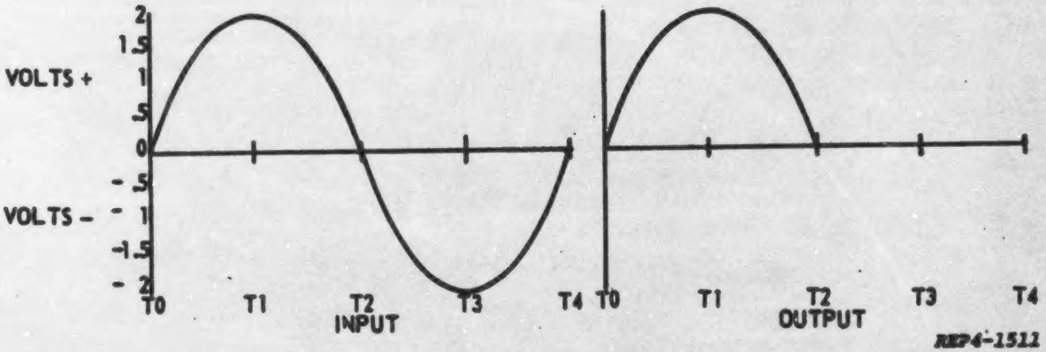
Graph 1-3

l. (1) shunt, positive

(2) no

(3) CR4

n.



REP4-1511

Graph 1-4

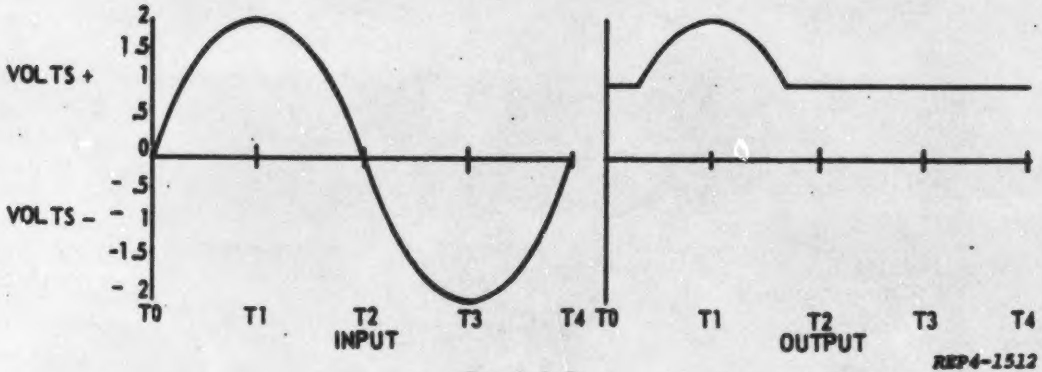
o. (1) shunt, negative, no

(2) CR3

r. Input 4 volts peak to peak

Output 1 volt peak

s.



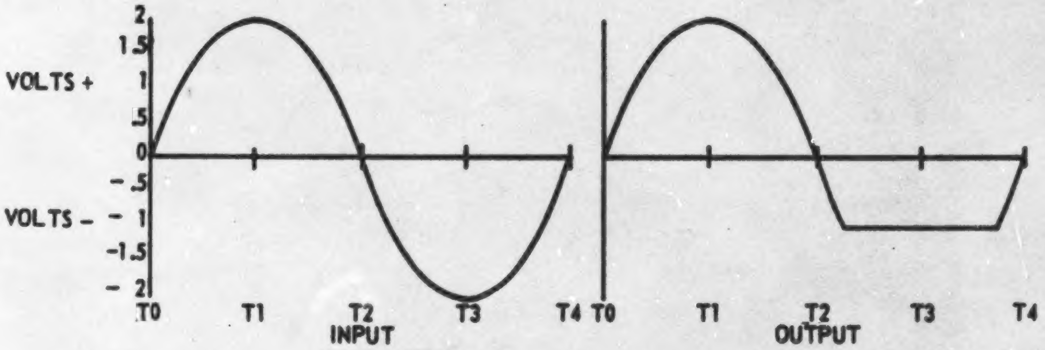
REP4-1512

Graph 1-5

t. (1) shunt, negative, positive

(2) negative, positive

w.



REP4-1513

Graph 1-6

x. (1) shunt, negative, positive

(2) True

z. The degree (amount) of limiting is primarily determined by the amplitude and polarity of voltage applied to the diode. Limiting will increase and decrease as bias is varied.

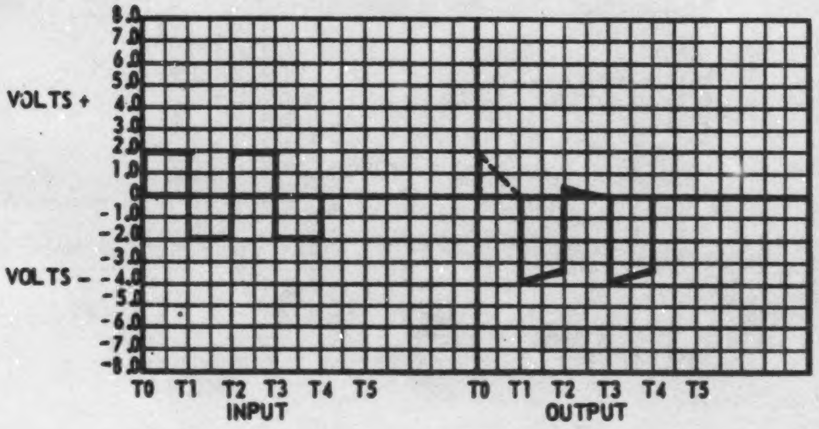
If your response to ANY of the statements is wrong or if ANY of your measurements are more than 10 percent different, go back and repeat that portion of the project. If necessary, review the referenced text material for clarification. Your instructor will assist if needed.

ANSWERS TO LAB EXERCISE 50-2:

3. d. Input 4 volts peak to peak

Output 4 volts peak

e.



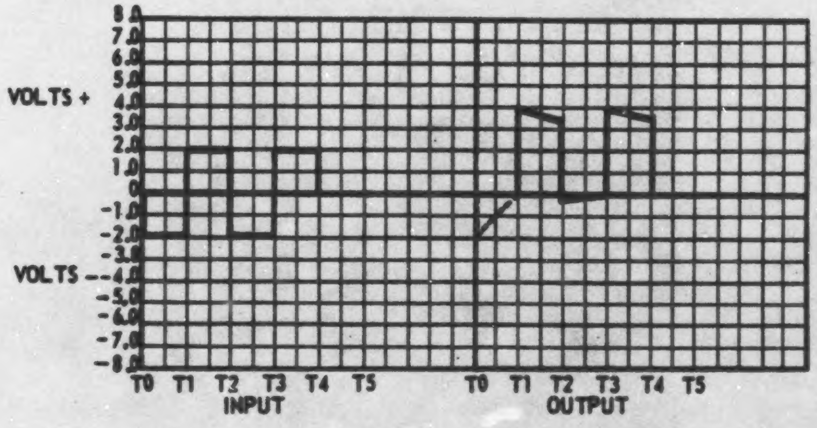
Graph 2-1

f. (1) negative, no
(2) charged, CR6
(3) C discharge slightly thru R4

g. (1) True
(2) 0 volts
(3) 0, decreased toward zero

h. (1) is
(2) decrease, faster, R4

j.

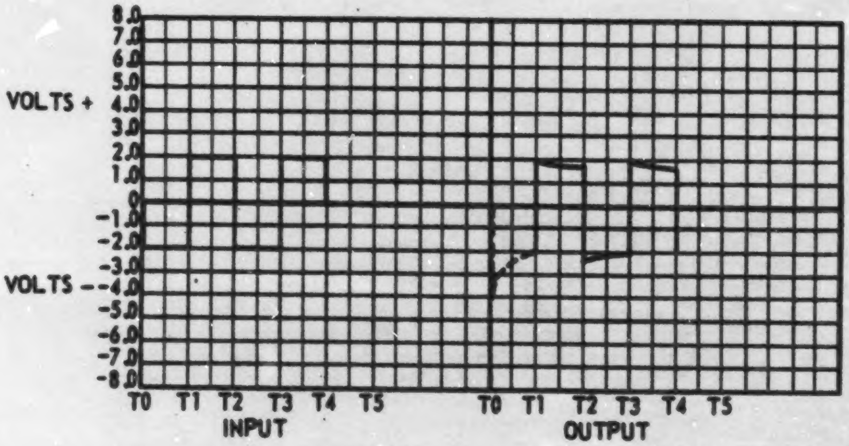


Graph 2-2

k. (1) positive, no

(2) 0, positive

m.

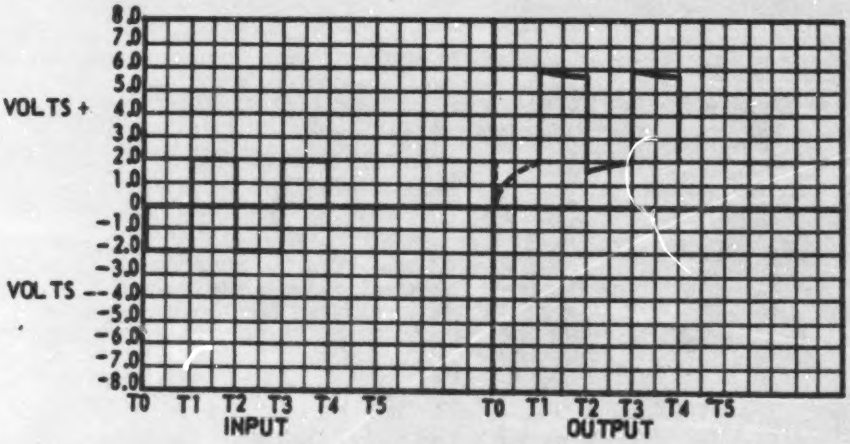


Graph 2-3

n. (1) positive, negative

(2) lower, -2

p.



Graph 2-4

q. (1) positive, positive

(2) lower, +2

r. (1) False

(2) True

(3) True

(4) True

If your response to ANY of the statements is wrong, or if ANY of your measurements are more than 10 percent different, go back and repeat that portion of the project. If necessary, review the referenced text for clarification. Your instructor will assist if needed.

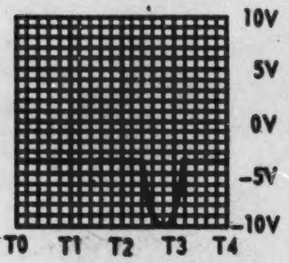
ANSWERS TO MODULE SELF-CHECK:

1. negative, one

2. parallel, an open

3. forward, reverse

4.

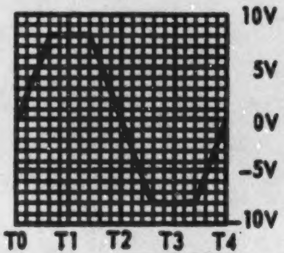


REP4-1525

5. positive, negative

6. double zener diode limiter

7.



REP4-1526

8. NPN, cutoff

9. decrease

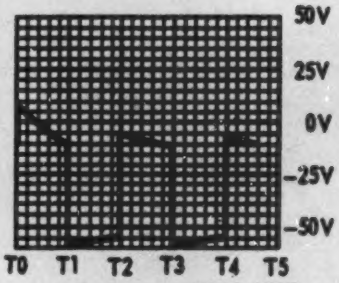
10. overdriven

11. c

12. lower, zero volts

13. negative, negative

14.



REP4-1527

HAVE YOU ANSWERED ALL OF THE QUESTIONS CORRECTLY? IF NOT, REVIEW THE MATERIAL OR STUDY ANOTHER RESOURCE UNTIL YOU CAN ANSWER ALL QUESTIONS CORRECTLY. IF YOU HAVE, CONSULT YOUR INSTRUCTOR FOR FURTHER GUIDANCE.